TOSHIBA

Service Training

NTDPJTV01

"Customer Satisfaction Through Knowledge"

SERVICING

PROJECTION

TELEVISION

TOSHIBA AMERICA CONSUMER PRODUCTS, INC.

"In Touch with Tomorrow"

FOREWORD

The material presented in this manual is for technical training purposes only.

Some of the circuits discussed are not utilized in all models.

The schematic diagrams included are simplified for training purposes and should not be used for actual troubleshooting.

Always refer to the proper service manual by model number whenever performing service or adjustments.

This material was prepared by the National Training Department of Toshiba America Inc.

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I.

INTRODUCTION

GENERAL INFORMATION

There are three new 7" cathode ray tubes inside Toshiba's giant 46" and 52" projection television sets, producing superior resolution and brightness thanks to a new type of phosphor that greatly improves radiation efficiency. Brightness now increases linearly in proportion to increased voltage, unlike the standard phosphor. In addition, the electron beams are accelerated to strike the phosphor harder. The results is a picture that is 25% to 30% brighter than conventional projection sets. A higher horizontal resolution of 560 lines has also been achieved through the new Electro Magnetic Focus System which replaces the conventional Static Focus System. A larger lens concentrates the electron beam, producing a spot that is 50% smaller and more intense. These changes are particularly impressive during the time of white peak. In addition, images are now just as sharp on the edges as they are in the middle, the result of a new Dynamic Focus System. As the beam scans from one edge...to the center...to the other edge, an adjustment is made in the lens that takes into account the distance between the lens and the screen surface.

The projection television uses the X-63G chassis which has a main PC board on which three PC boards are vertically mounted. The function of each board is listed below.

* PIF and SIF Board
* CCD Comb Filter
* MTS Board

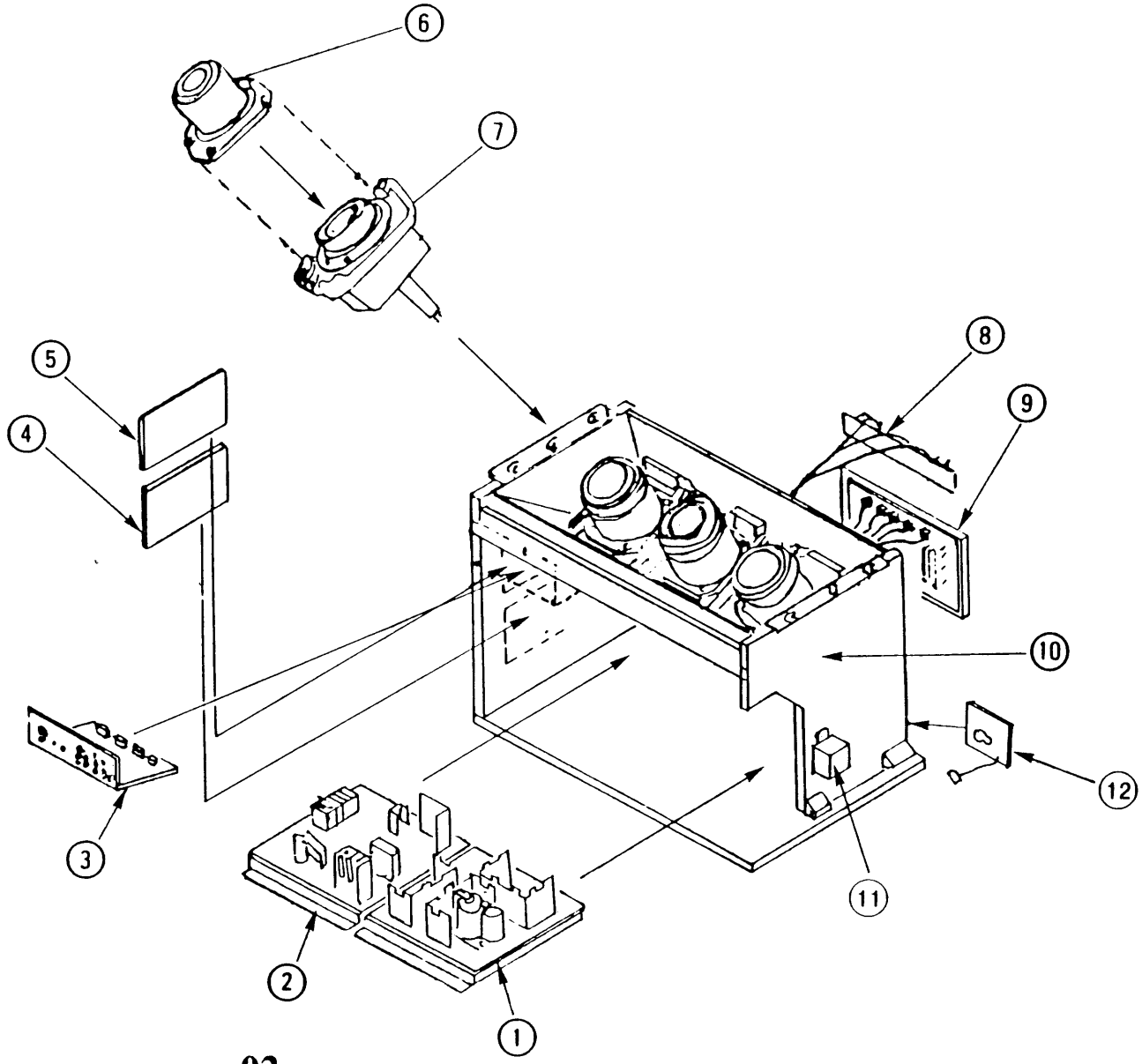
In addition, there are the following PC boards which are mounted throughout the cabinet.

* Carver Audio Board
* Audio/Video Board
* PIP Board
* Power Supply Board
* Convergence Board
* CRT Drive Boards (3)

Should any modifications be required in the future, they will be made to the individual PC boards.

CHASSIS CONSTRUCTION

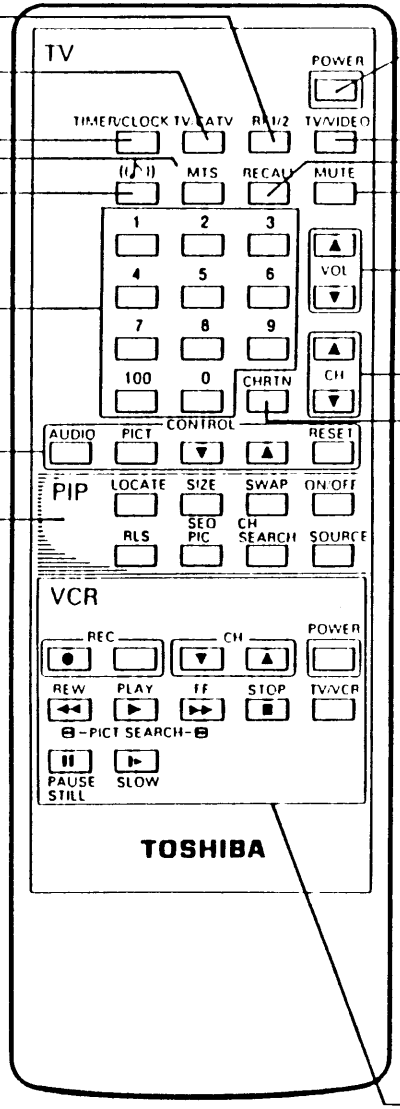
1) POWER PCB
2) MAIN PCB
3) A/V INPUT PCB
4) CARVER AUDIO PCB
5) PIP PCB
6) MAIN LENS
7) CRT ASSEMBLY & OPTICAL COUPLING (R) (G) (B)
8) FRONT CONTROL PANEL
9) CONVERGENCE PCB
10) LIGHT BOX
11) POWER TRANSFORMER
12) CRT DRIVE PCB (R) (G) (B)



FEATURES AND SPECIFICATIONS

	MODELS	
	TP4648	**TP5288**
Screen Size	46"	52"
Viewing Angle	H: 120 /V: 20	H: 120 /V 20
Horizontal Resolution	560 Lines	560 Lines
Peak Brightness Level	>300 foot-lambert	>300 foot lambert
Hybrid Lens System	yes	yes
Optical Coupling System	yes	yes
Channels	181	181
RF Inputs	2	2
Unified Remote	50 key	50 key
PIP	1/4 & 1/16	1/4 & 1/16
PIP Swap	yes	yes
PIP Still	yes	yes
PIP Position Change	yes	yes
PIP Channel Search	4 Channels	4 Channels
PIP Sequential picture	4 Frames	4 Frames
Peak-ACL/ABCL	yes	yes
Off-Timer	180 min. max.	180 min. max.
Program Scan	yes	yes
Comb Filter	CCD	CCD
A/V In/Out	2-A/V In, 1-A/V Out	2-A/V In, 1-A/V Out
S-VHS Input	yes	yes
Var. Audio Out	yes	yes
Audio Output	12W	12W
Surround Audio	Carver	Carver
MTS (STR/SAP/MONO)dbx	yes	yes
On-Screen Display	yes	yes

REMOTE CONTROL HAND UNIT



* RF1/2 button
Press to select either the RF-1 or RF-2 mode.

* TV/CATV button
Press to select either the TV or CATV mode.

* TIMER/CLOCK button
Press to set to the clock setting mode or time setting mode.

MTS button
Press to select the Stereo, SAP or Mono mode.

SONIC HOLOGRAM button
Press to select the Sonic Holography mode.

* CHANNEL NUMBER button
Directly select channels you want.

Audio and Picture control buttons

* Picture In Picture control buttons

POWER button
Press to turn the TV set on.
Press again to turn off.

TV/VIDEO button
Press for playback from the external equipment connected to "VIDEO 1" or "VIDEO 2" jacks.

* RECALL button
Press to display the time and channel number on the screen.

* MUTE button
Press to cut off the sound.
Press again to resume normal sound.

VOLUME UP ▲ /DOWN ▼ buttons
Press UP ▲ button to increase volume.
Press DOWN ▼ button to decrease volume.

CHANNEL UP ▲ /DOWN ▼ buttons
Press UP ▲ button to scan up.
Press DOWN ▼ button to scan down.

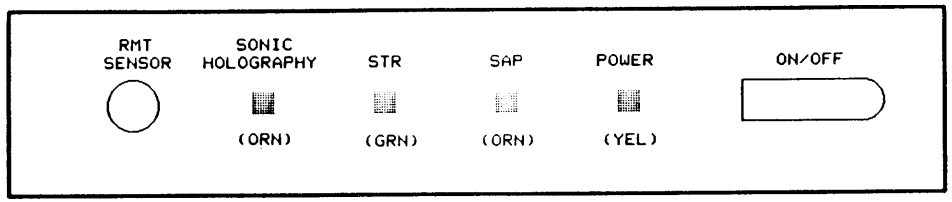
* CH RTN button
Press to switch the last channel previously tuned.
Press again to return to the present channel.

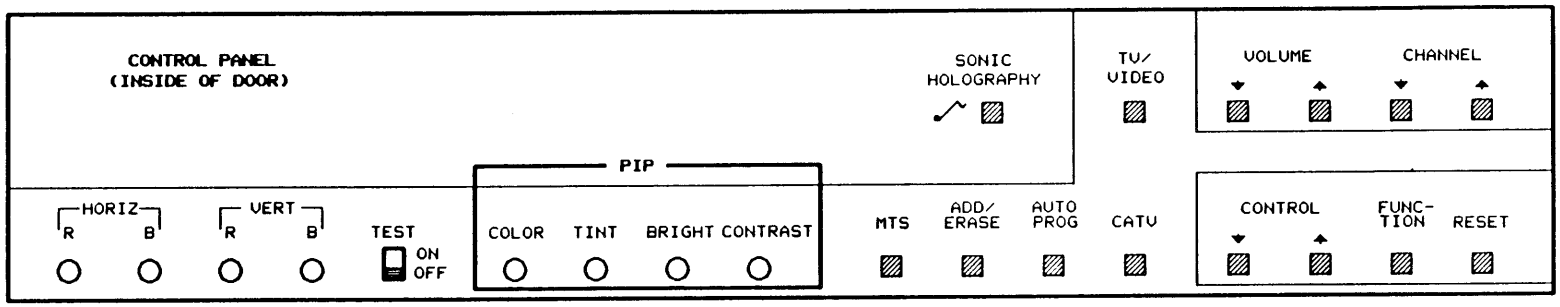
* VCR function buttons

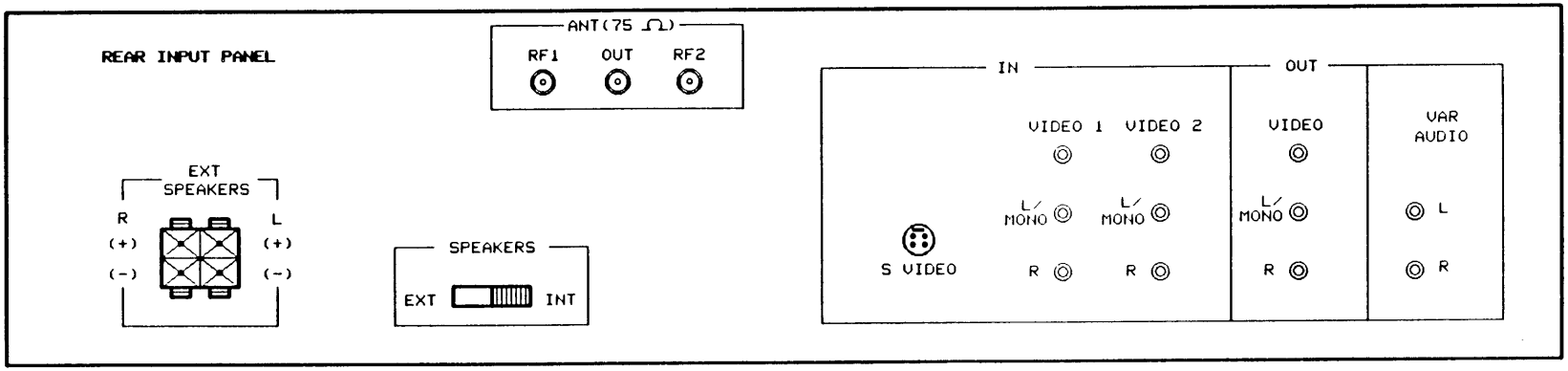
* These functions do not have duplicated locations on the TV set. They can be controlled only by the Remote Control Hand Unit.

FRONT AND REAR CONTROLS

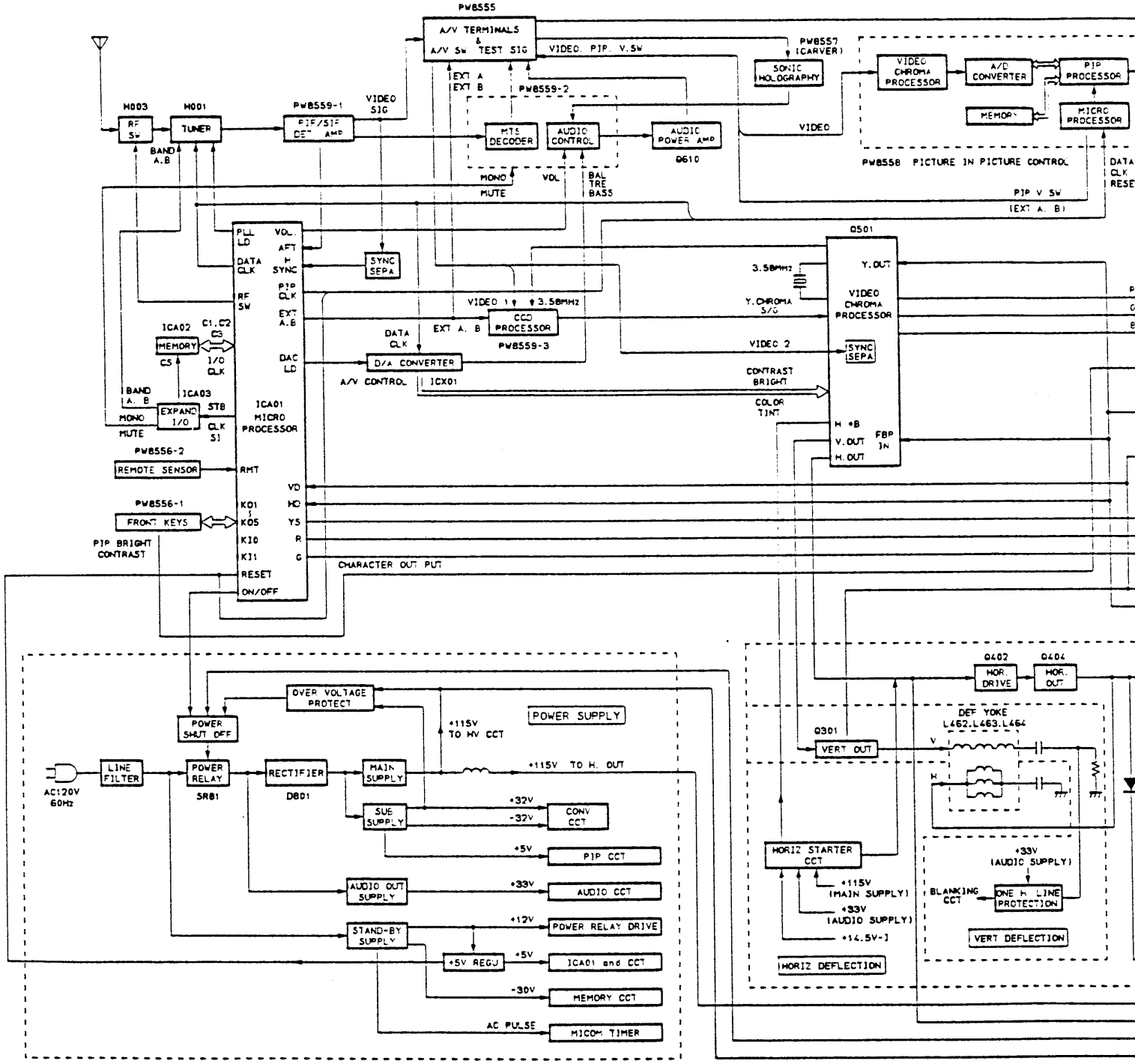
FRONT CONTROL DISPLAY

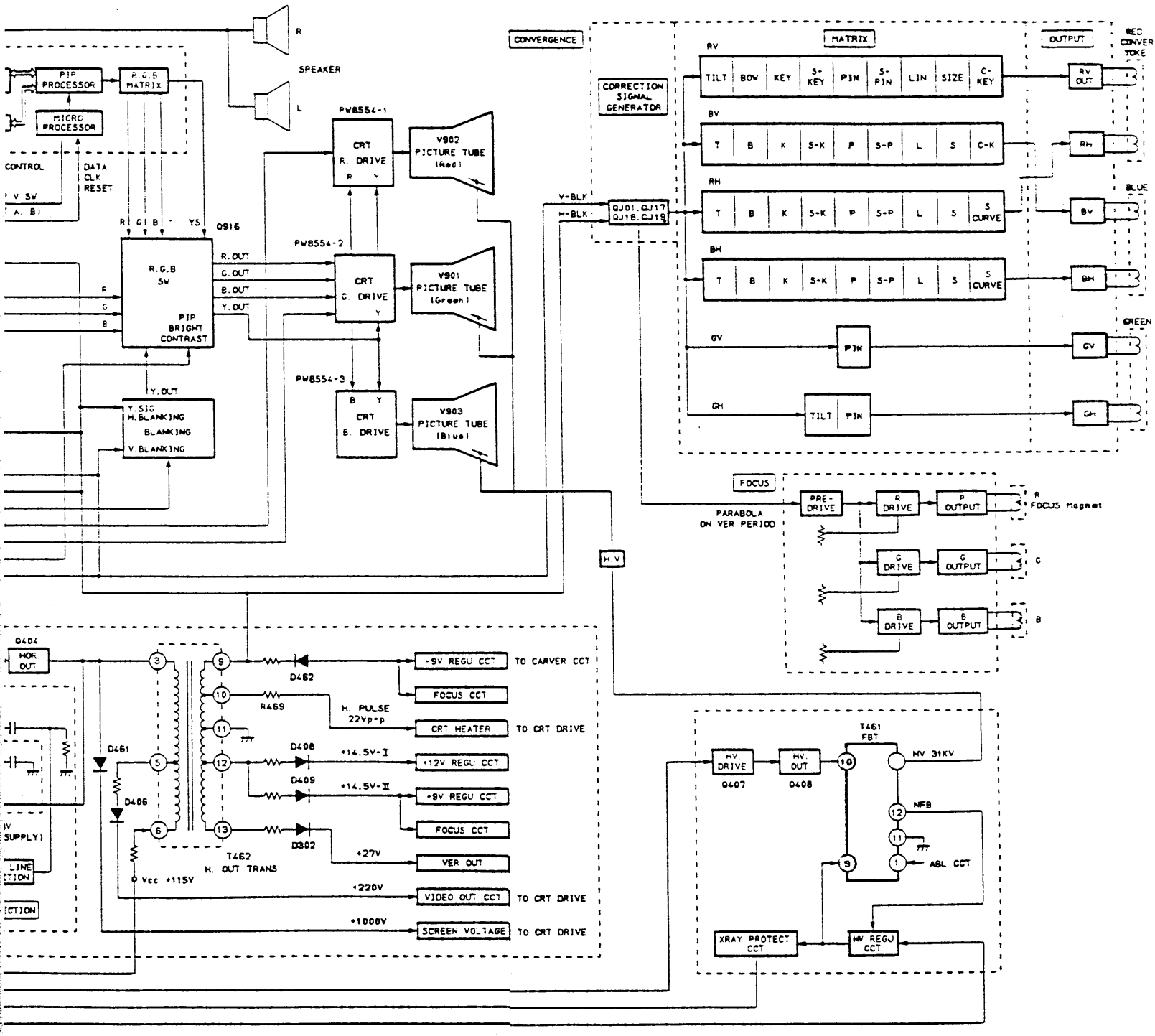






CIRCUIT BLOCK DIAGRAM




R
SPEAKER
L
PIP PROCESSOR
R.G.B MATRIX
MICRO PROCESSOR
CONTROL
DATA
CLK
RESET
PW8554-1
CRT R. DRIVE
V902 PICTURE TUBE (Red)
R G B YS
Q916
R.G.B SW
PIP BRIGHT CONTRAST
R.OUT
G.OUT
B.OUT
Y.OUT
PW8554-2
CRT G. DRIVE
V901 PICTURE TUBE (Green)
PW8554-3
CRT B. DRIVE
V903 PICTURE TUBE (Blue)
Y.SIG
H.BLANKING
BLANKING
V.BLANKING
CONVERGENCE
CORRECTION SIGNAL GENERATOR
V-BLK
H-BLK
QJ01, QJ17
QJ18, QJ19
MATRIX
OUTPUT
RV
TILT
BOW
KEY
S-KEY
PIN
S-PIN
LIN
SIZE
C-KEY
RV OUT
BV
T
B
K
S-K
P
S-P
L
S
C-K
RH
S CURVE
BH
GV
GH
FOCUS
PRE-DRIVE
R DRIVE
P OUTPUT
PARABOLA ON VER PERIOD
G DRIVE
G OUTPUT
B DRIVE
B OUTPUT
H.V
Q404
HOR. OUT
D462
R469
H. PULSE 22Vp-p
D461
D406
D408
D409
D302
T462
H. OUT TRANS
-9V REGU CCT
FOCUS CCT
CRT HEATER
+14.5V-I
+12V REGU CCT
+14.5V-II
+9V REGU CCT
FOCUS CCT
+27V
VER OUT
+220V
VIDEO OUT CCT
+1000V
SCREEN VOLTAGE
TO CARVER CCT
TO CRT DRIVE
TO CRT DRIVE
Vcc +11.5V
T461 FBT
HV DRIVE
Q407
HV OUT
Q408
HV 31KV
NFB
ABL CCT
XRAY PROTECT CCT
HV REGU CCT

II.

POWER SUPPLY

POWER SUPPLY CIRCUITS

The power supply circuits for the TP4688 and TP5288 are mounted on the POWER SUPPLY PC BOARD and consists of the following 4 power supplies:

(1) The Standby Power Circuit (Switching Type).
This power circuit will provide the "Keep-alive" Voltages. -30V to the Non-volatile Memory Circuit, +5V for the uP and Remote Circuit and provides reset to the uP. Also, +12V is supplied to the power relay.

(2) The Main Power Circuit (Switching Type).
This power circuit provides the +115V to both the Horizontal Output Circuit in the Main PCB, and the H V Circuit in the Power PCB.

(3) The Sub-power Circuit (Switching Type).
This power circuit provides the +/-32V to the Convergence Circuit and +5V for Picture In Picture Circuit.

(4) The Audio Out Power Circuit (Linear Type).
This power circuit provides +33V for the Audio Circuit and Horizontal Start-up. It consists of the power transformer T864 (mounted on right side of light box) and the bridge rectifier circuit on the PS Board.

In addition, several scan-derived supplies are provided by the fly-back transformer T462 of the Horizontal Deflection Circuit. These voltages are covered in the Horizontal Output section of this manual.

Starting at the AC input is the Rectifier Circuit (See Fig.1). Here the AC supply voltage is filtered by T801/T802 and coupled to T864 of the Audio B+ Circuit. One leg of the AC supply is rectified by diodes D820/D821 and filtered by C820. This DC output is supplied to the Stand-by Power Circuit. Another leg of the AC supply goes through power relay SR81 and on to the AC input terminals of the bridge rectifier block D801. The rectified output from D801 is filtered by C810 and supplied the Main and Sub-Power Supply Circuits.
R810 will limit any current surges that will occur when the unit is turned ON.

RECTIFIER CIRCUIT

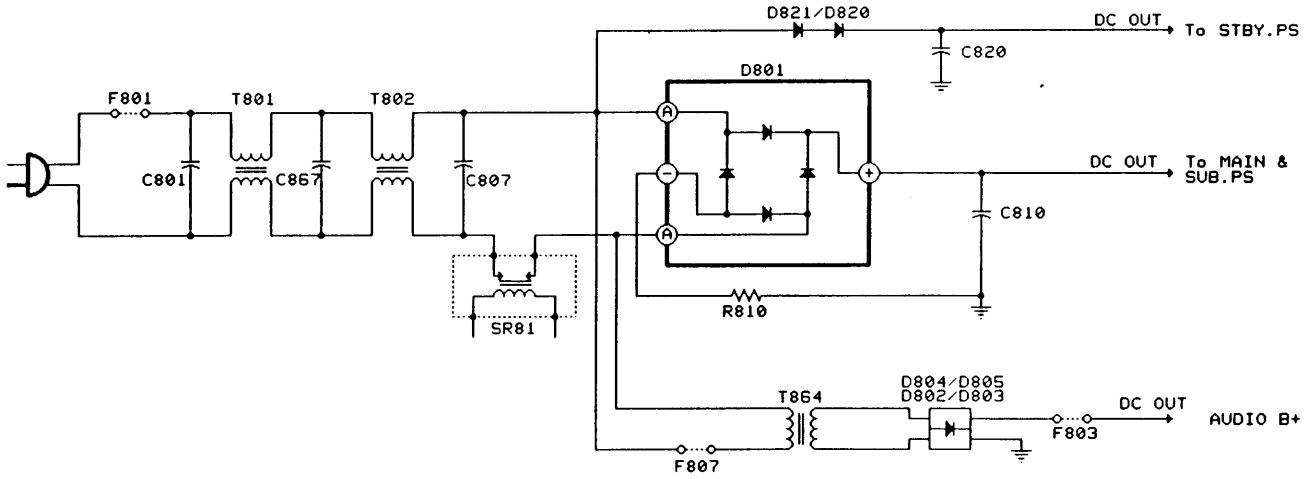


FIG. 1

THE STANDBY POWER SUPPLY

The Standby Power Supply provides the "Keep-alive" Voltages. They include +12V to the Power Relay, +5V to the Main Microprocessor IC & Remote sensor as well as -30V to the Memory IC. Reset to the Main uP is also developed here.

The Standby Power Supply Circuit consists of a Self-excited Converter type ringing choke which uses a Hybrid IC (STR-D1005) as the Switching Regulator IC. D820, D821 and C820 work as a half wave rectifier circuit and develop the Input DC voltage. Also, a rectified AC pulse from D821 is supplied to the photo-coupler IC820 which produces an AC pulse that is used in the timer operation of the Microcomputer.

When the Input Voltage is applied to IC802 pin 2, Q1 Base Current flows through start-up resistor R822 and Q1 turns ON. Now the Input Voltage will flow through the primary winding (NP) of transformer T840, into IC802 pin 3, through Q1, to ground. This induces a voltage through the secondary winding (NB). This induced voltage causes current to flow through C822, into IC802 pin 1, through D2 and back out through pin 5. This current also flows up through R2 to the base of Q1, which increases the base current (IB) of Q1 further, and finally IB will reach a constant value, (saturation point). At the same time the collector current (IC) of Q1 will increase proportionally with time. This current increase however can not be maintained after a time when IB<IC. As a result, the voltage across the NP winding ceases to increase thereby stopping the build-up of magnetic flux and causing a decrease in voltage across the NB winding. The decrease in voltage across the NB winding is going to decrease the current flow up through R2 to the base of Q1. Now the base current (IB) decreases and Q1 is turned off rapidly. At the moment that Q1 is turned off, reverse EMF (with the polarity inverted) occurs on each winding of the transformer. The energy stored in the transformer is the same as it was just before Q1 was turned off. This energy is supplied to the load.

STANDBY POWER SUPPLY CIRCUIT

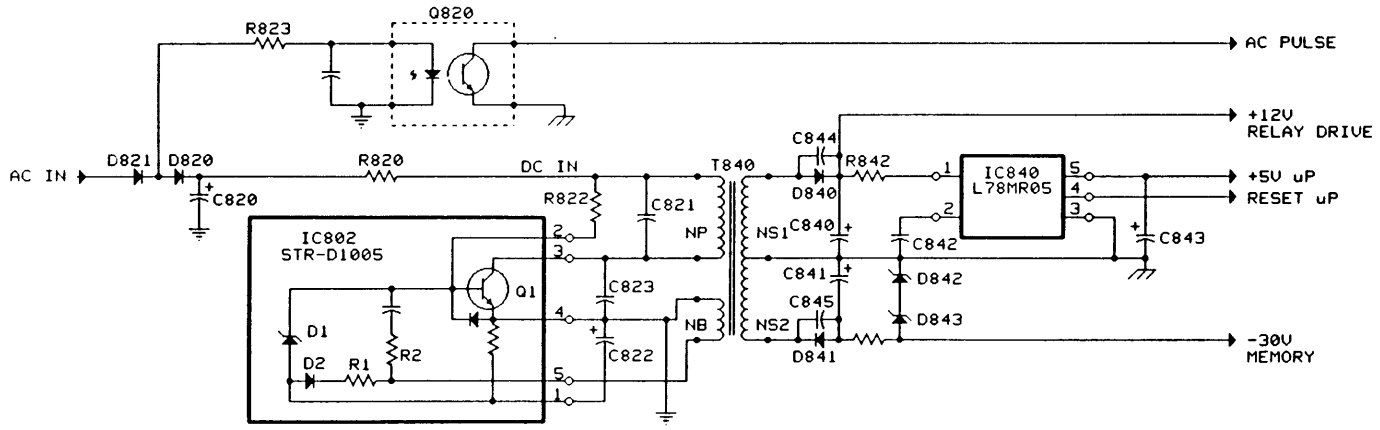


FIG. 2

STANDBY POWER SUPPLY (CONT.)

During Q1's off period, C822 is charged through D2 from the NB winding, and this voltage will be negative. It will cause D1 to conduct and the base current (IB) will flow towards D1, thereby keeping Q1 off.

Furthermore, the period in which current is flowing into C822 is the same as the period in which the secondary coil of T840 is supplying power to the output circuit. The voltage at the secondary (VO) is proportional to the charge voltage (VC) at C822. This is how voltage regulation is performed. If the output voltage goes up, this increase will cause an increase of current flow on the secondary winding (NS), the current flow at NB will also go up, but because the NB winding is inverted, the current flow will be negative. This negative current flow will be felt at the anode side of D1 causing it to conduct ahead of time which in turn will turn off Q1 faster than normal. This causes the duty cycle of NP to be shorter, which in turn will lower the voltage on the secondary side. If the output voltage was to go down, the above procedure will take place in reverse.

Notice that on this particular power supply, theoretically the frequency is not adjustable. Only the duty cycle is adjustable.

On the secondary side of T840, Capacitors C844, and C845 are used to prevent spurious diode radiation. D840 & C844 make up a +12V rectifier circuit. D841 & C845 make up a -30V rectifier circuit.

R842, and IC840 (voltage control IC L78MR05) are part of a DC/DC Converter, which provides the uP +5V & the initial reset.

STANDBY POWER SUPPLY CIRCUIT

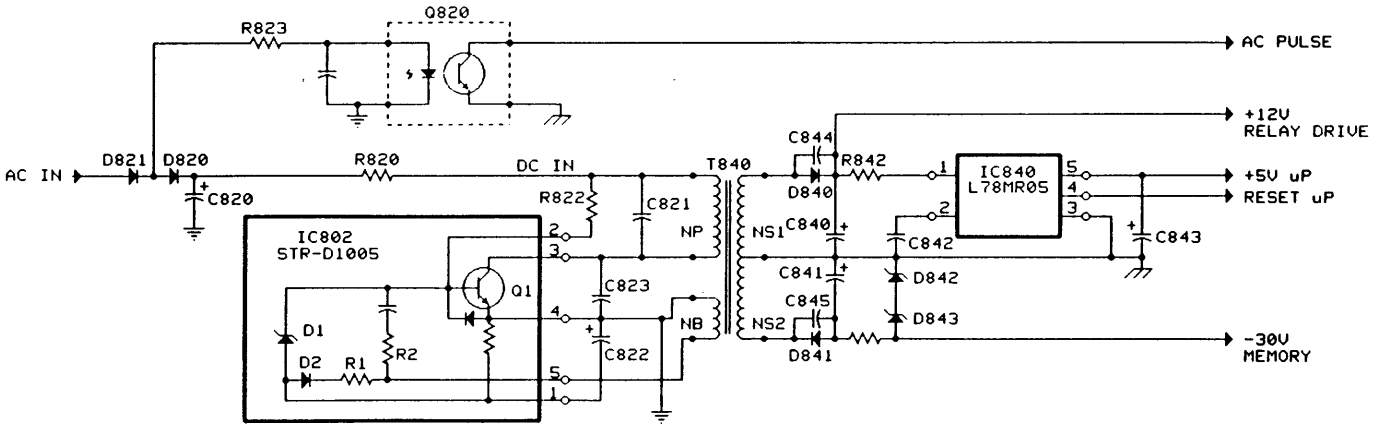


FIG. 2

THE MAIN POWER SUPPLY

The Main Power Supply provides 115V output to the Horizontal Output Circuit on the Main Board, and to the High Voltage Output Circuit on the PS Board. This power supply is called an "Automatic Voltage Regulator".

The Main Power Supply Circuit, like the Stand-by Power Circuit, consists of a Self-excited Ringing Choke Type Converter. It uses a Hybrid IC (STRS5041S) for a Switching Regulator IC801.

When the Input DC Voltage is applied to IC801 pin #3, Q1 base current (IB) flows through the Start Up Resistor R862 and Q1 turns ON. During the Q1 ON period, current flows through the Primary Winding (NP) of the Transformer T862. Then a voltage with the opposite polarity as the Primary Winding (NP) will be induced on the Secondary Drive Winding (NB). As a result, C866 will be charged through a loop made up of D1, C866, D2, and R861. While Q1 is in the ON period, Q3 is forward bias by the charge stored in C869 which is rectified by D2 and applied to the voltage divider of R1/R2, so now Q1 base current will flow from C866, through Q3, and R867. This causes Q1 to coduct very hard towards saturation. When the Base Current (IB) reaches a specified value which is proportional to the Input Voltage (E in), the collector current (IC) would have reached Q1's saturation point. Now the voltage across the primary winding (NP) ceases to increase thereby stopping the buildup of magnetic flux and causing a drop in voltage across the secondary winding (NB). The voltage drop across the NB Winding will reduce the base current of Q1 and thus Q1 is turned OFF. Now the energy stored in T862 is transferred to the output load. When the current supplied to the load falls to zero, the voltage across the winding of T862 develops a ringing voltage. The same kind of voltage will also be induced in the Drive Winding (NB). When the ringing voltage changes from zero to the next half cycle, a recovery current at the Diode D863 flows and this allows a forward bias to flow through the Q1 Base-Emitter instantly. With this biasing operation, Q1 will turn ON again. Hereafter, the same operations are repeated, thus oscillation will continue.

Accordingly, if the AC Line voltage drops, causing the voltage across the NB Winding to drop, a constant base current will be supplied to Q1 during the ON period from the charge stored in C866. So C866 helps to stabilize the oscillation by determining the time constant, which it does by boosting the collector voltage of Q3.

MAIN POWER SUPPLY CIRCUIT

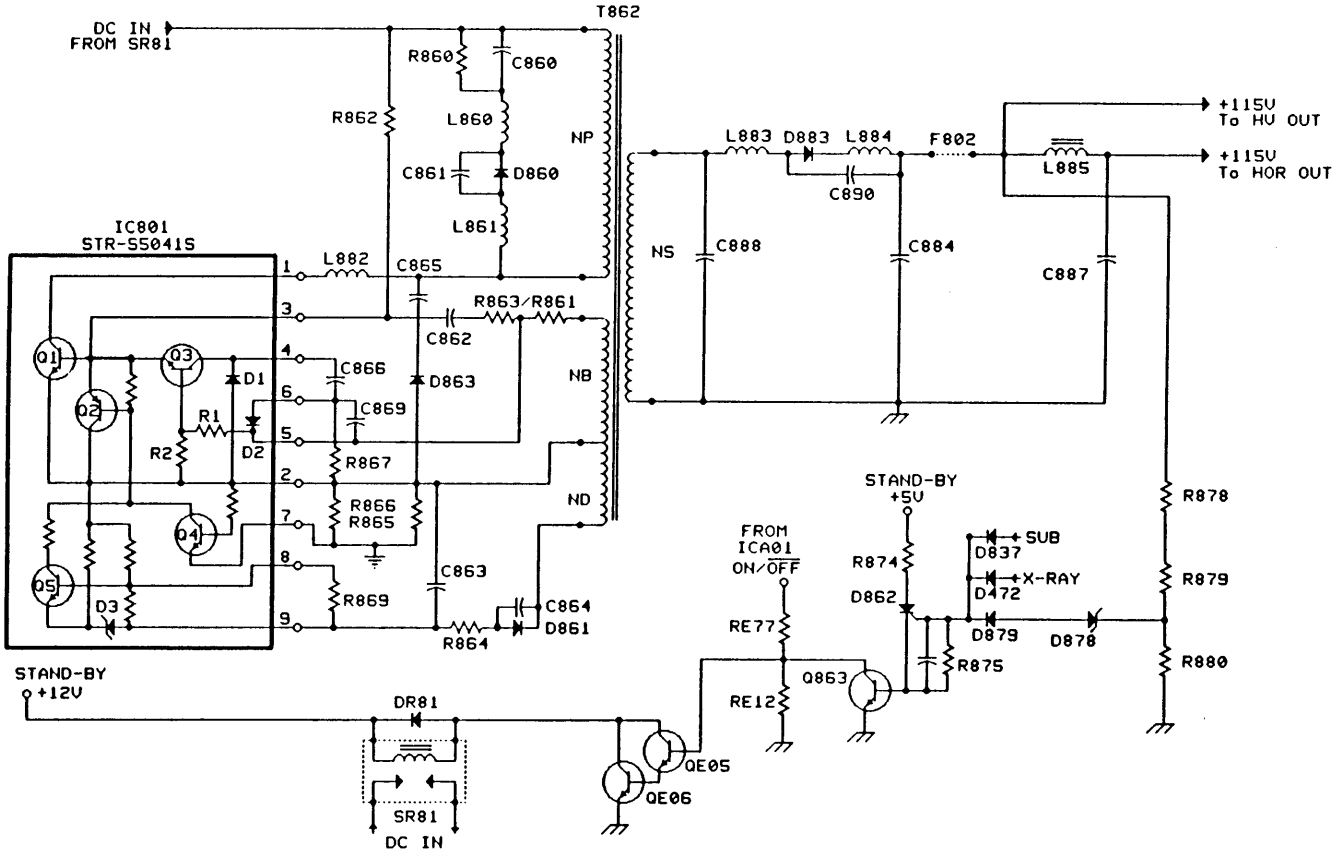


FIG. 3

MAIN POWER SUPPLY (CONT.)

The ND Winding (Detection Secondary Coil) and the NS Winding is provided to control the stability of the power supply. D861, R864, and C863 work as a rectification circuit and develops a Detection Voltage of -42 volts. When the secondary voltage increases, the voltage across the secondary detection coils also increases. This will increase the voltage across C863 (-42V line) which will turn ON D3 and depending on the value of R869 will turn ON Q5 which in turn will turn ON Q2. This will Cut-Off Q1, thus stabilizing the output voltage with a shorter ON cycle. This is the Voltage Monitor Operation.

The Q1 Collector Current outputs from pin 2 of IC801 and flows into R865/R866 (Monitor Resistors). In the event that the current goes high, Q4 is turned ON through an internal resistor, turning Q2 ON and cutting OFF the base of Q1. At this time the output voltage will drop. This is The Over Current Protection Circuit.

THE SECONDARY CIRCUIT

D883, C884, L883 and L884 rectify and filter the +115V Out to the Horizontal Output and the HV Output Circuits.

R878, R879, and R880 are Over Voltage Detection Resistors. Zener Diode D878 and Thyristor D862 work as Over Voltage Protectors. During normal operation, QE05-QE06 (Darlington configuration) are turned ON by the "Turn ON" Signal from the Microprocessor. This will supply a path for the +12V from the Stand-by Power Supply which will energize the Power Relay. If the +115V line increases excessively (15%), D878 will turn ON causing D862 to also turn ON. This will send +5V from the Stand-by Power Supply, through D862, to Q863. This will turn ON Q863 and the "Turn ON" signal from the Microprocessor will go to ground, thereby turning OFF QE05-QE06 and de-energize the Power Relay. Because the +5V line from the Stand-by Power Supply will continuously supply a current to the Thyristor D862, this Power Relay Shut-Off Operation will be held until the AC Power is disconnected. D862 will also turn ON if the output voltage of the Sub-power Circuit rises abnormally (detected by D837) or when the X-Ray Protection Circuit is actuated (detected by D472).

MAIN POWER SUPPLY CIRCUIT

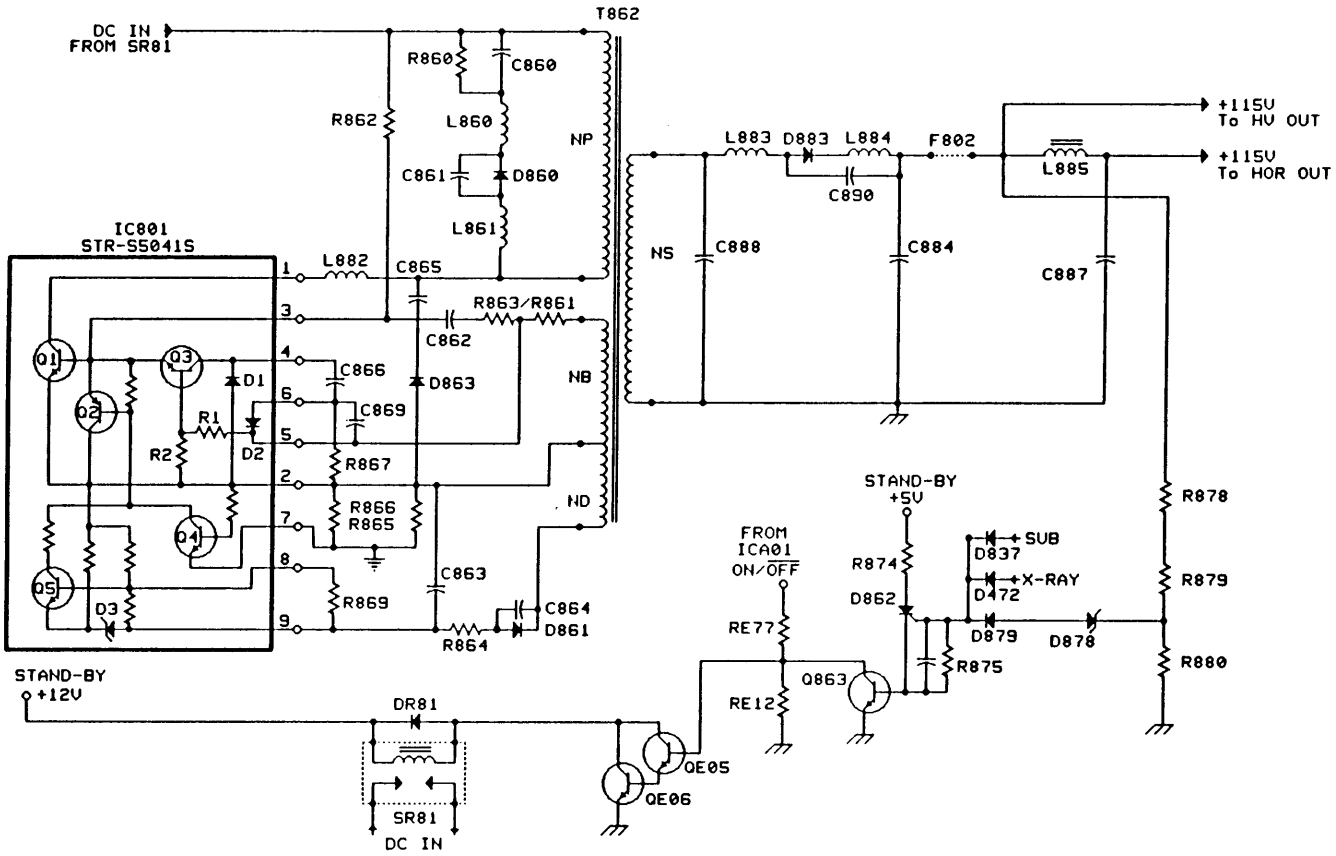


FIG. 3

SUB-POWER SUPPLY CIRCUIT

The Sub-power Supply Circuit produces +/-32V to be supplied to the Convergence Circuit Board, and +5V to be supplied to the PIP Circuit Board.

The limited availability of power that can be taken from the Main Power Supply Circuit is the reason why a Sub-power Supply Circuit is provided totally independent of the Main Power Supply Circuit. The Sub-power Circuit is a switching power supply made up of discrete components, but the basic principle of operation is identical to that of Standby and Main Power Supply Circuits.

Circuit discription is as follows;

Across the primary winding of T863, components D831, C833, and R833 make up a clamping circuit that will suppress any voltage spikes. R830 is the start-up resistor and Q803 is the main switching transistor. Q805 and D833 make the Q803 base current bypass circuit that will control the stability of the power supply. R831 and Q804 perform the over current protection operation.

On the secondary side of T863, the output of winding Ns2 goes through D834/C837 and make up the +32V rectifier circuit. The output of winding Ns3 goes through D835/C838 and make up the -32V rectifier circuit. Furthermore, the +32V source will be divided by R837 and R838 and then applied through D836,D837 to the gate of thyristor D862 for over voltage protection.

The output of winding Ns1 goes through D838/C848 and make up a +8V rectifier circuit. The +8V goes through a regulation circuit made up of Q806, D809 and C807. This will output +5V.

SUB-POWER SUPPLY CIRCUIT

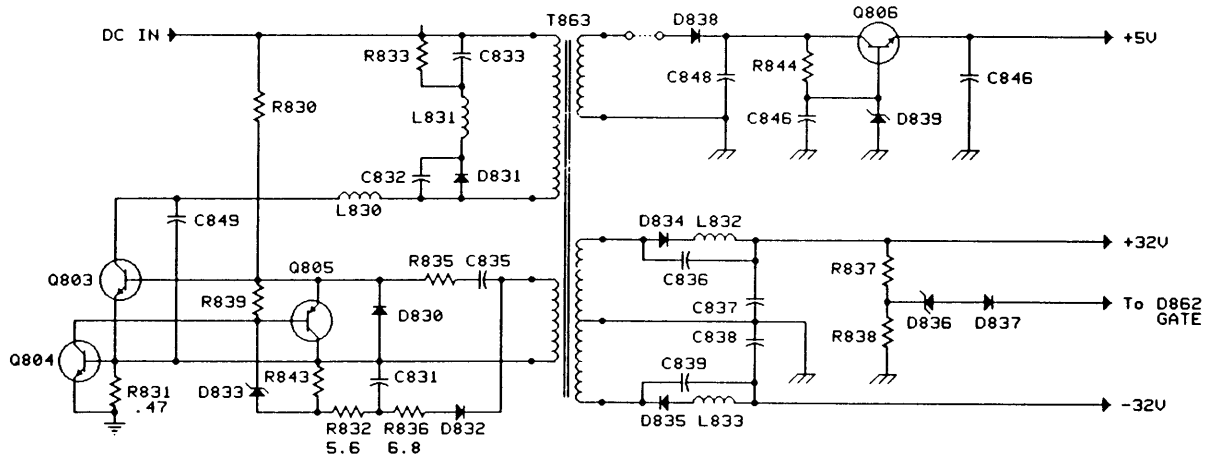


FIG. 4

NOTES

III.

SYSTEM CONTROL

TUNING SYSTEM

The projection TV tuning system performs frequency synthesized tuning and controls all TV set operations by using a newly developed single chip 4-bit microcomputer containing a built-in on-screen display character generating circuit.

A diagram of the tuning system is shown in the block diagram below (Fig. 1).

Principal Features:

(1) Nominal channel capacity is 181 Channels (VHF, UHF, mid, super, hyper and ultra bands of CATV).

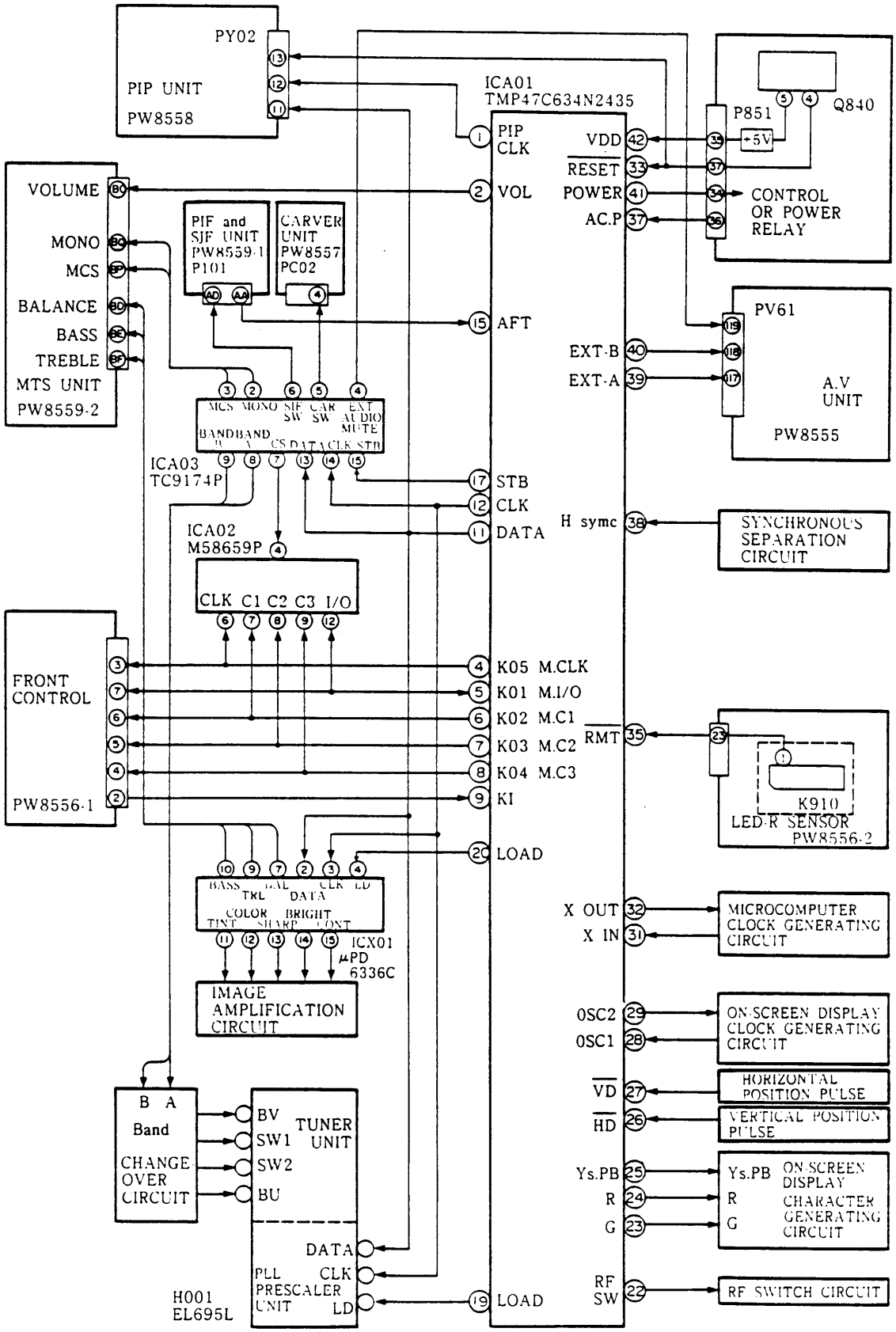
(2) A D/A Converter IC (ICX01) is utilized to perform the audio/video digital control, thereby improving the performance of the circuit.

(3) A microcomputer with a built-in on-screen display character generating circuit is adopted to perform the on-screen display, making the system compact.

(4) System control of PIP operation is provided.

(5) A port expansion IC (TA917P) has been adopted to up-grade the system.

BLOCK DIAGRAM OF TUNING SYSTEM



TUNING SYSTEM (Cont)

Tuning Control Microcomputer

A newly developed microcomputer (TM47C634N2435) having an on-screen display character generating circuit is used as the tuning control microcomputer. This microcomputer controls the entire system of the set as described below with priority given to the tuning process:

(1) Front control panel input detection
(2) Remote control transmitter input detection
(3) Power ON/OFF
(4) Audio and video digital control
(5) Volume control
(6) Carver ON/OFF
(7) Multi-voice switching
(8) Mute
(9) Clock OFF timer
(10) RF input switching
(11) On-screen display control
(12) PIP circuit control
(13) Audio/video input switching
(14) Port expansion IC control
(15) Non-volatile memory control
(16) CATV switching
(17) Auto program, add/erase
(18) Tuning process (10 keys, channel up/down)

Pin names and functions of the microcomputer are shown (Fig. 2).

TUNING CONTROL MICROCOMPUTER

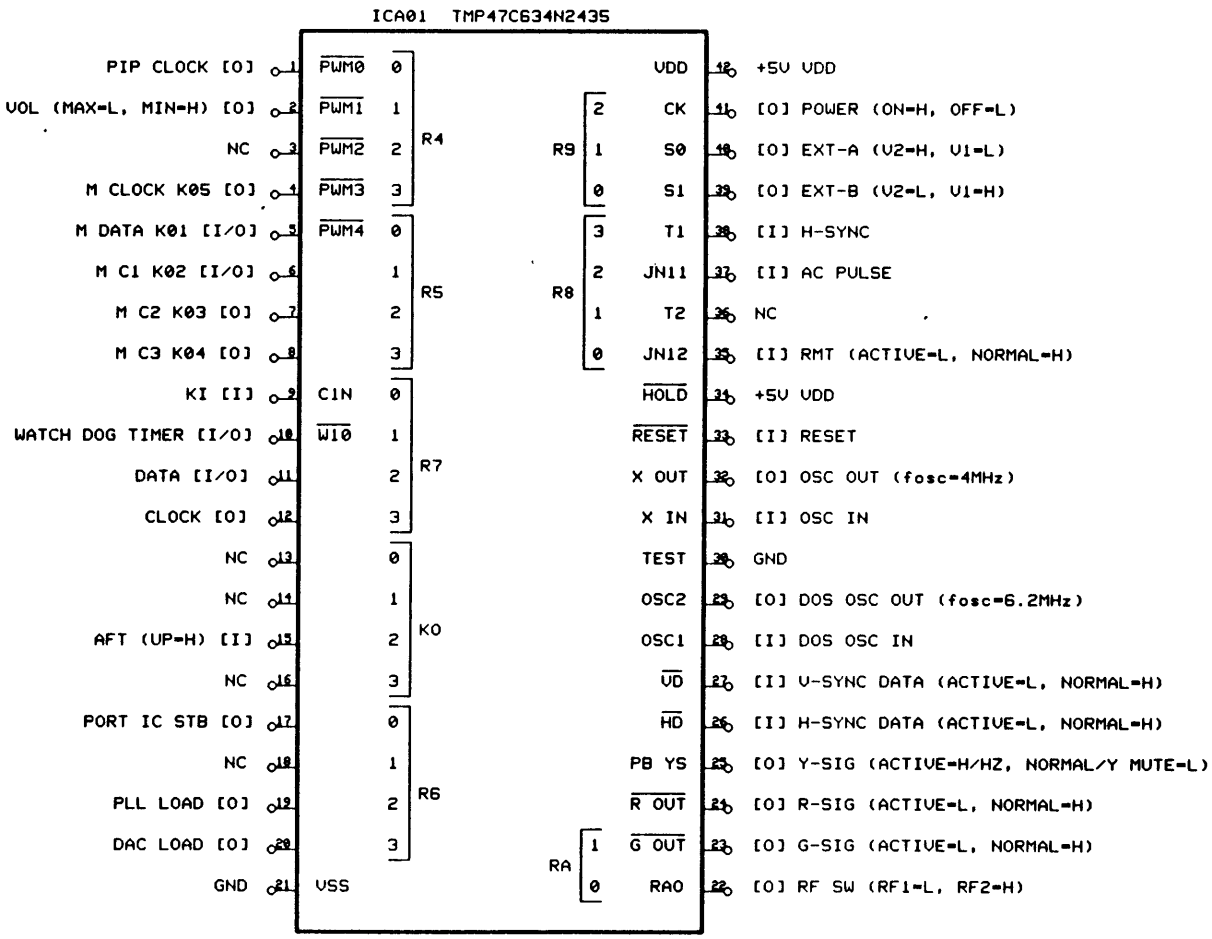


FIG. 2

TUNING SYSTEM (Cont)

Description of Tuning System Circuit Operation

Front control panel input detection:

When key button switches on the front panel are pushed (see names of key button switches below), voltages obtained through voltage dividing resistors (R1-R5), shown in Fig. 3, input Pin 9 of the microcomputer. The circuit inside the microcomputer consists of a 3-bit D/A converter and a comparator. Variations of the input voltage level at Pin 9 of the microcomputer are detected by comparing it with the reference voltage and the output voltage from the 3-bit D/A converter.

As shown in Fig. 3, the key input detection is performed at five input blocks. For instance, if a key button is checked at Pin 8 (Block 1), Pin 8 of the microcomputer is held at earth potential and Pins 7 through 4 are in the floating state (at high impedance). This step is repeatedly carried out in order from Pins 8 to 4 of the microcomputer. If no key buttons are pushed, Pin 9 of the microcomputer is at +5V.

Timing Waveform

SA01	POWER	SA06	VOL UP	SA12	CARVER ON/OFF
SAO2	TV/VIDEO	SA07	VOL DN	SA15	AV FUNCTION
SA03	MTS	SA08	PROGRAM	SA16	AV RESET
SA04	CH UP	SA09	CATV	SA17	AV UP
SA05	CH DN	SA19	ADD/ERASE	SA18	AV DN

KEY INPUT DETECTION CIRCUIT & TIMING WAVEFORM

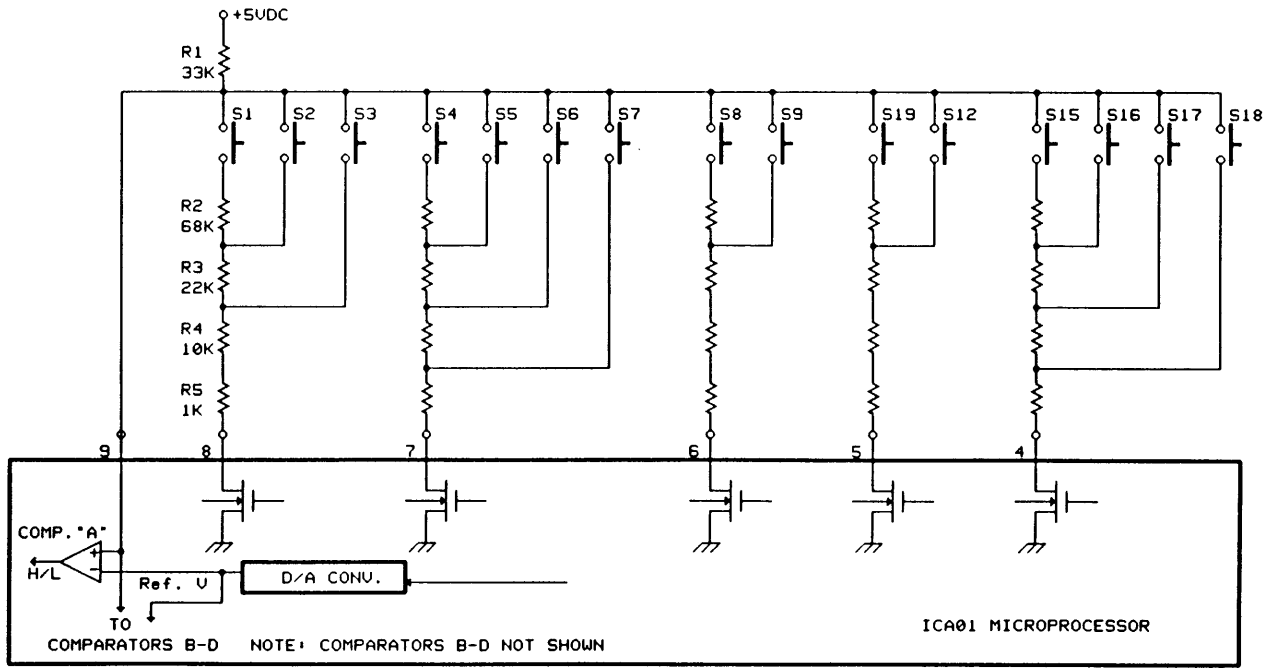
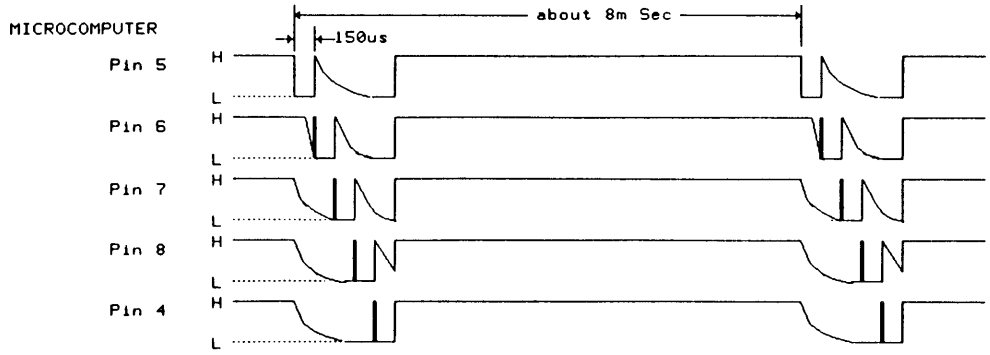


FIG. 3



AUDIO/VIDEO DIGITAL CONTROL

Audio/Video digital control is performed through the Digital to Analog Control (DAC) ICX01 (uPD6336C) by the Microcomputer (ICA01).

The **contrast, brightness, sharpness, color and tint** are controlled in the video circuit, while **bass, treble and balance** are controlled in the audio circuit. As shown in Fig. 4, the microcomputer transfers digital signals serially through three output terminals (DATA, CLOCK and LOAD) to the input interface circuit of the DAC IC.

The DAC IC latches the data and converts it into an analog signal by a ladder-type resistor group which has 64 step (6-bits) resolution, and outputs control voltages from pins 7 through 15. This DC control at pins 7 through 15 can vary from about 0 volts to about 9 volts. Furthermore, in order to assure a stable operation of the DAC, the microcomputer will update the data periodically or if changes are made through the remote control.

D/A TERMINAL LOGIC

Pin No. uPD6336C	Signal	Terminal Name	Functions
1	Vcc	Interface Power Supply	Interface power supply for external control (Microcomputer, etc). Voltage same as the controller power supply.
2	DATA IN	Serial Data Input	Data are read in synchronization with rising edge of the shift clock signal applied to input terminal of the control data and clock terminal.
3	CLOCK	Shift Clock Input	Clock terminal for data reading. Date applied to DATA IN terminal of the IC are read in at rising edge of the clock signal.
4	LOAD	Load Pulse Input	Strobe input after serial data entry. When high level pulse is applied to LOAD terminal, data are latched in data latch of the D/A converter and in data latch of the option output.
7	DA_8	D/A converter output 8	D/A converter output 8. D/A converter output range is GND through VDD.
9-15	DA_7-DA_1	D/A converter outputs 7-1	D/A converter outputs 7 through 1
16	V_{DD}	D/A Reference Power Supply	Reference power supply (+) for D/A converter.

DAC CONTROL CIRCUIT & TIMING WAVEFORM

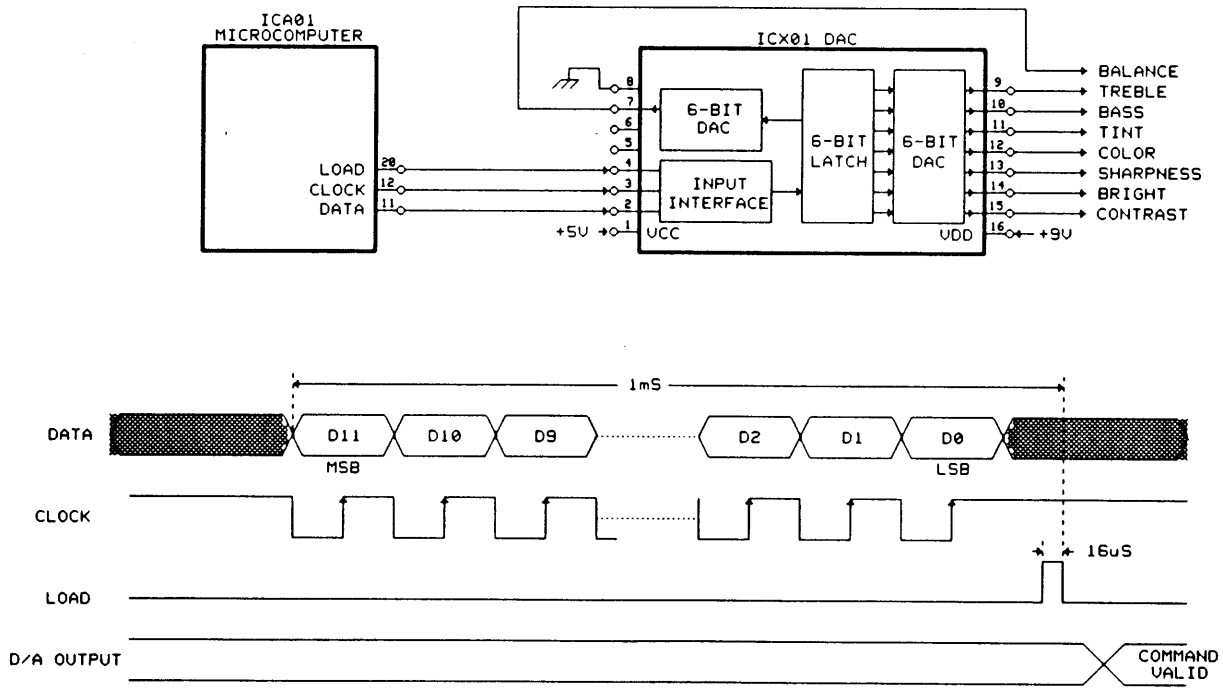


FIG. 4

NON-VOLATILE MEMORY

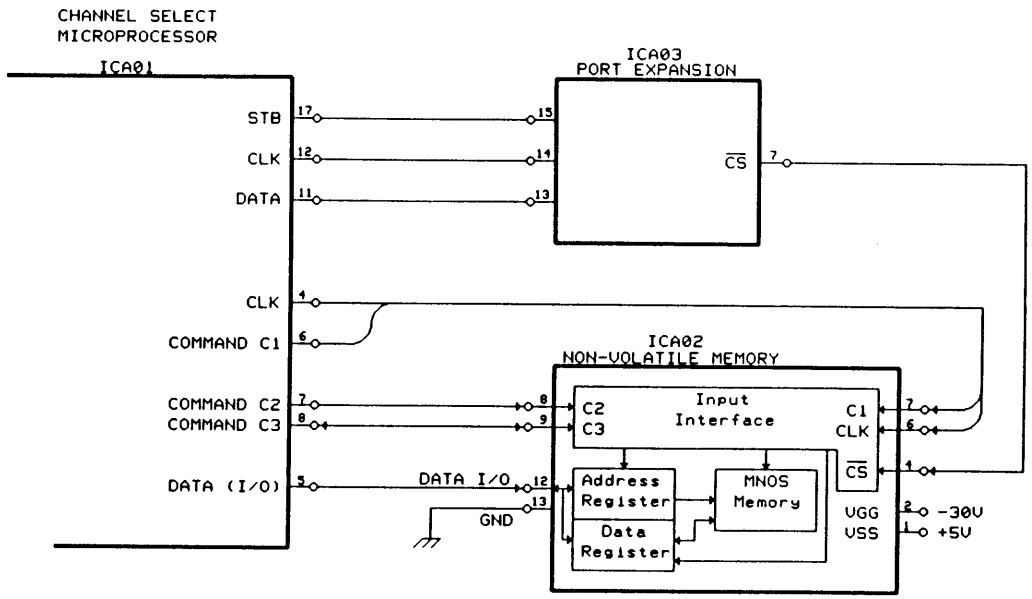
The non-volatile memory ICA02 (M58659P) stores "last data" information such as Ch No., volume, color, etc. that is needed to return the TV system to the original state should the AC power be disconnected. To memorize the last data on items listed below, the channel select microcomputer is always reading and writing to the non volatile memory. This updates the data when operations are conducted through the remote control or by the key switches on the TV set. This non-volatile memory has a memory capacity of 512 bits and stores the data described below:

(1) All Channel Memory
(2) Power Source
(3) CATV Mode
(4) RF Input
(5) Last Ch
(6) Audio/video Digital Control
(7) Carver
(8) Volume

As shown in (Fig. 5), Data, Mode Change Pulses, and Clock Pulses output from pins 4 through 8 of the microcomputer to pins 6 through 9 and 12 of the non-volatile memory IC. Pin 5 of the microcomputer also serves as the input pin when reading data from the non-volatile memory.

The Microcomputer controls the Port Expansion IC which in turn will output a Chip Selecting (CS) Signal through pin 7 to pin 4 of the Non-volatile Memory IC. The CS Signal will go "Low" during Data Write In/Data Readout. The Mode Change Pulses along with the Clock Pulses feed into the Input Interface of ICA02 and will toggle the memory between Data Read/ Write & Standby. The Data will be writing into the memory as Address Data (12-bit) and Input Data (16-bit). The control circuit of the Non-volatile Memory IC and the memory control timing waveforms are shown in the timing chart in the nexy page.

NON-VOLATILE MEMORY CONTROL CIRCUIT



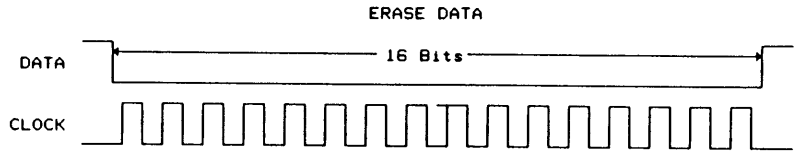
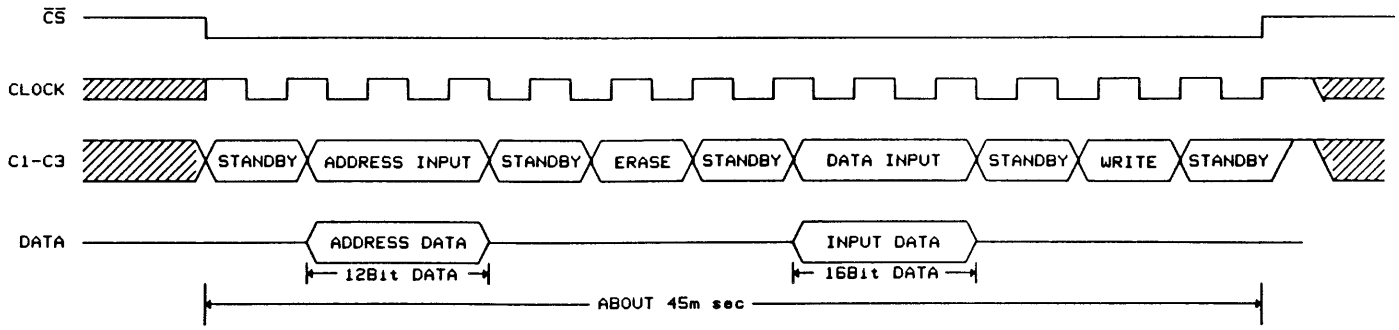
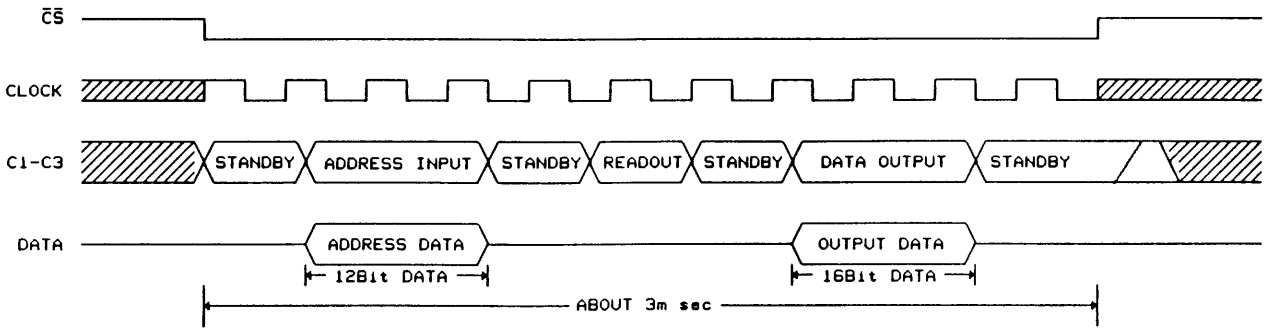


FIG. 5

READ/WRITE TIMING WAVEFORM



WRITE DATA (CH SELECT uP -> MEMORY)



READ DATA (MEMORY -> CH SELECT uP)

C1	C2	C3	FUNCTIONS
H	H	H	STANDBY-address and contents of data register are held. Output buffer enters floating condition.
H	H	L	DUMMY-not used.
H	L	H	ERASE-contents of memory transistor in address designated by address register is erased. The erase is equivalent to write "L" on all bits (16) at the designated address.
H	L	L	ADDRESS INPUT- I/O terminal data is transfered to address register & the address register is set. With this mode, 20 words address can be designated.
L	H	H	READOUT-contents of memory transistor at the address designated is transferred to data register.
L	H	L	DATA OUTPUT-contents of data register is output in synchronization with the clock.
L	L	H	WRITE-contents of data register is written on memory transistor at address designated by the address register.
L	L	L	DATA INPUT-I/O terminal write data is read in the data register. Contents of the address register is held.

CONTROL OF PORT EXPANSION IC

The purpose of the Port Expansion IC is to increase the control of the Microcomputer (ICA01) over the entire system.

Output ports of the Port Expansion IC (ICA03: TC9174P) are controlled by the Microcomputer through three control lines. These control lines are: DATA (Address Data [12 bit] and Output Data [16 bit]), CLOCK & STB.

In order to assure stable operation of the Port Expansion IC the microcomputer will update the data to the Port Expansion IC periodically or every time operations are conducted through the remote control or by key switches on the TV set. The control circuit of the Port Expansion IC is shown in Fig. 6.

Contents of the Port Expansion IC outputs:

(1) Multi-voice Mode Switching
(2) Carver ON/OFF
(3) Ext Audio Mute
(4) SIF Switching
(5) Band Switching
(6) Non-volatile Memory "CS Signal" output

PORTS OUTPUT LOGIC TABLE

MULTIVOICE MODE SWITCHING

	STEREO	SAP	MONO
MCS (#3)	H	L	H
MONO (#2)	L	L	H

SIF SWITCH

		ICA03 #6
SIF	ON	H
SWITCH	OFF	L

CARVER ON/OFF

		ICA03 #5
CARVER	ON	H
	OFF	L

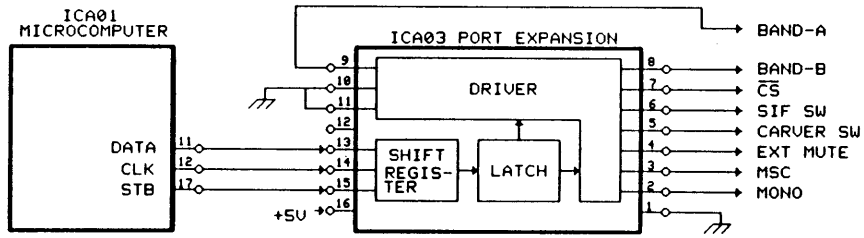
EXT AUDIO MUTE

		ICA03 #4
EXT AUDIO MUTE	ON	H
	OFF	L

BAND SWITCHING

CATV	VL	VH	VH	HYPER	UHF
TV	VL	VH	---	---	UHF
BAND-A #8	L	L	H	H	H
BAND-B #9	L	H	H	H	L

PORT EXPANSION IC CONTROL CIRCUIT & TIMING WAVEFORM



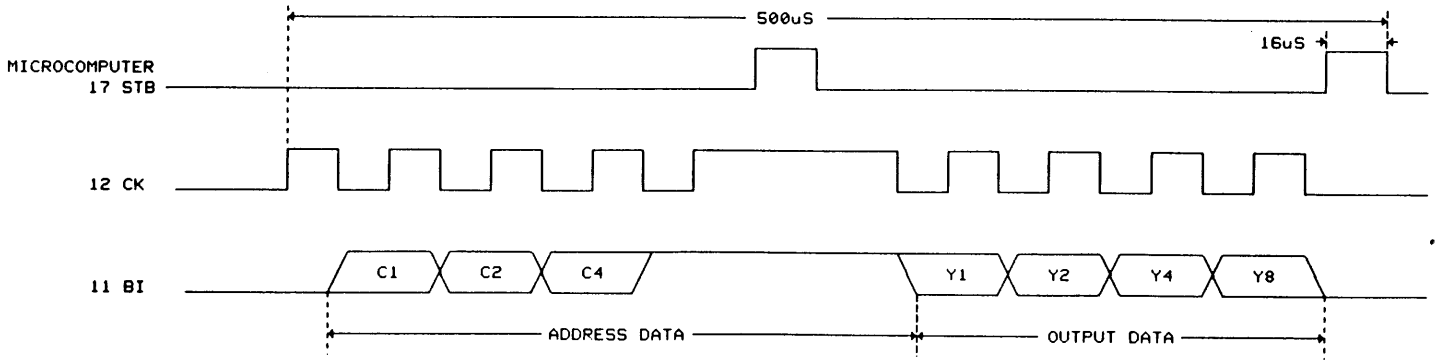


FIG. 6

CONTROL OF A/V SWITCHING

The A/V Signal Switching Circuit's function is to switch incoming video and audio signals of the antenna and external inputs. This is performed at ICV01 (TA7717P) in the A/V Circuit. ICV01 is controlled by the Microcomputer (ICA01) through two control lines (EXT-S & EXT-B), see Fig. 7. TV, VIDEO 1/S-VIDEO, and VIDEO 2 are switched in the order shown by the logic table below. Video/audio outputs are also provided along with a Variable Audio Out.

ICA01	TV	VIDEO 1	VIDEO 2
EXT-A (#39)	H	L	H
EXT-B (#40)	H	H	L

THEORY OF OPERATION

The detected video from IC101, enters the A/V Board and inputs switching ICV01 at pin 15. The input video signals (E1/S-Video and E2) enter ICV01 at pins 7 and 11 respectfully. The selected video will output at pin 25 and input ICS22 (Test Signal SW IC), through a clamp circuit and amp (QV12, 13 & 14). The signal now outputs the A/V Board and is coupled directly to the CCD Circuit. The chroma signal of the S-Video input is directly coupled to the S-Video switching circuit ICV40 on the CCD Board.

The TV Audio Signal (Lch, Rch) and each of the input audio signals (E1 & E2) also input ICV01 (see A/V Switching Block Diagram) and the selected input is coupled to the TV A/V Out and to the Carver PCB.

A/V SWITCHING CONTROL CIRCUIT

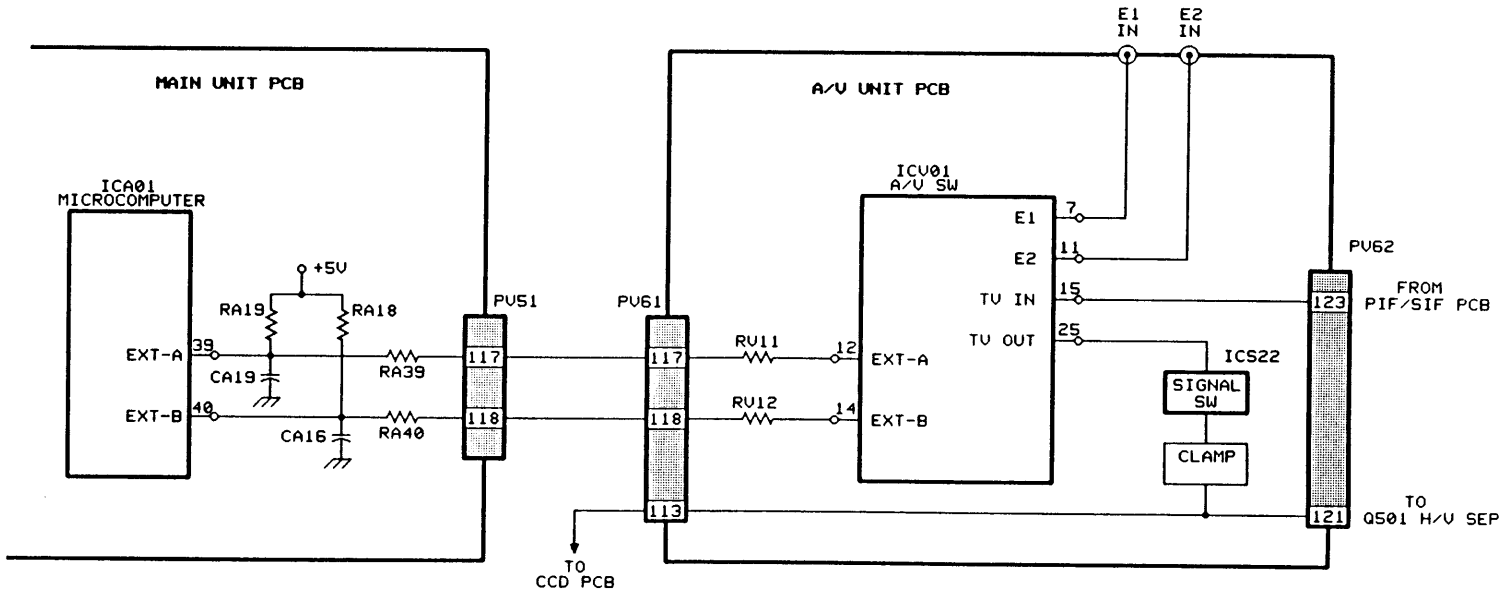


FIG. 7

ON-SCREEN DISPLAY CIRCUIT

The On-screen Display Character Generator is contained within in and controlled by the microcomputer. It manipulates (by a program) the display of characters, display position, character sizes, character colors, display ON/OFF, and so forth. The generated signals output ICA01 through pins 23, 24, and 25. They are, Ys (positive logic), R (non-logic) and G (non-logic) Signals. The On-screen Display Circuit is shown in Fig. 8.

Contents of the On-screen Characters Display are;

(1) Ch # (RF-1)
(2) RF-2 Ch #
(3) MUTE
(4) VIDEO 1 or 2
(5) VOLUME
(6) CATV CH # & MODE (STD,HRC,IRC)
(7) MTS MODE (STR,SAP,MONO)
(8) TIMER/CLOCK
(9) A/V DIGITAL Control
(10) PIP Source

The On-Screen Display Circuit requires three control signals: CLOCK, HD and VD.

The Clock Generator consist of the Oscillator IC (LA02). It inputs a 6.2MHz signal to pins 28 and 29 of ICA01, which is controlled by HD. The free run (HD=OFF) frequency of this oscillation circuit is 6.2 MHz.

VD (V sync Data) is needed to determine the vertical position of the on-screen display. The Vertical Sync Pulse outputs from the pulse amplifier at Q301 (AN5521) pin 6 of the Vertical Output Circuit. The signal is coupled through QB20 for polarity inversion and is applied to the microcomputer at pin 27.

HD (H sync Data) is needed to determine the horizontal position of the On-screen Display. The Horizontal Sync Pulse is taken from Pin 9 of the FBT (T462). The signal is inverted through QB21 and is applied to the microcomputer at pin 26.

ON-SCREEN DISPLAY CIRCUIT

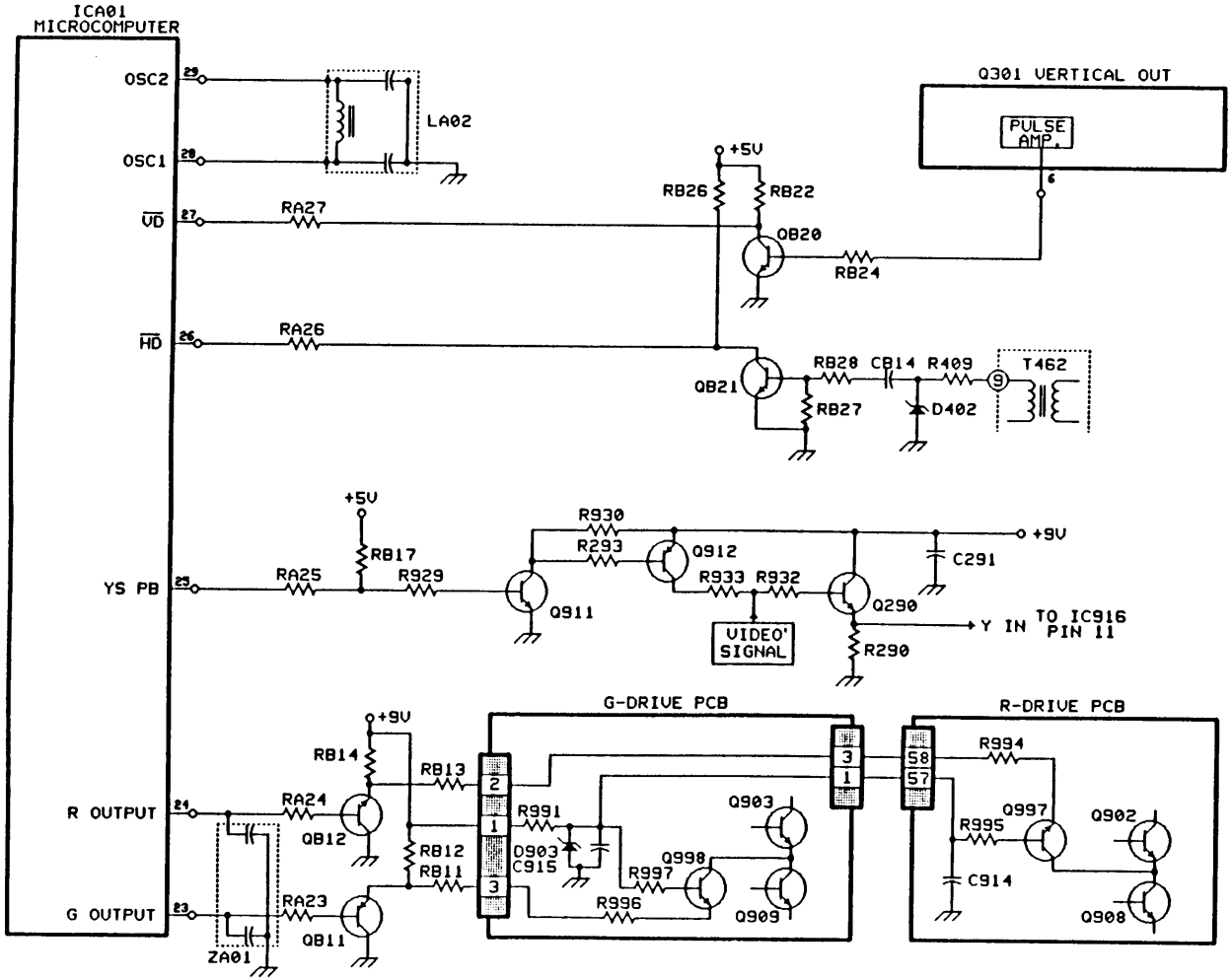


FIG. 8

ON-SCREEN DISPLAY CIRCUIT (Cont)

The Ys Signal is a positive logic signal (H Active) during On-screen Display. It is output from pin 25 of the microcomputer and cuts off the video signal by turning ON Q911 and Q912.

Additionally, since picture blanking is needed during "Power ON" and "Channel Selection", the Ys signal is also used during this time.

During on-screen display, the R Signal outputs the microcomputer through pin 24 and is resistance coupled to the base of QB12. The emitter of QB12 is connected to the emitter of Q997 through RB13 and R994 in the R-Drive PCB. The base of Q997 is supplied with a constant voltage of about 4.3V from the G-Drive PCB, and the collector of Q997 is connected to the intersecting point of Q902 and Q908 in the CRT drive circuit. As a result, when the R signal outputs from Pin 24 of the microcomputer, QB12 is turned ON. Accordingly, Q997 is turned ON and current flows to QB12 from Q997 through R994 and RB13, and the R signal from the On-screen Display Circuit is superimposed on the R-CRT Drive Circuit.

The G Signal output circuit has the same circuit configuration as that of the R Signal output circuit. When the G Signal outputs from Pin 23 of the microcomputer, QB11 is turned ON. As a result, Q998 of the G-Drive PCB is turned ON and current flows to QB11 from Q998 through R996 and RB11. Now the G Signal from the On-screen Display Circuit is superimposed on the G-CRT Drive Circuit.

ON-SCREEN CONTROL CIRCUIT

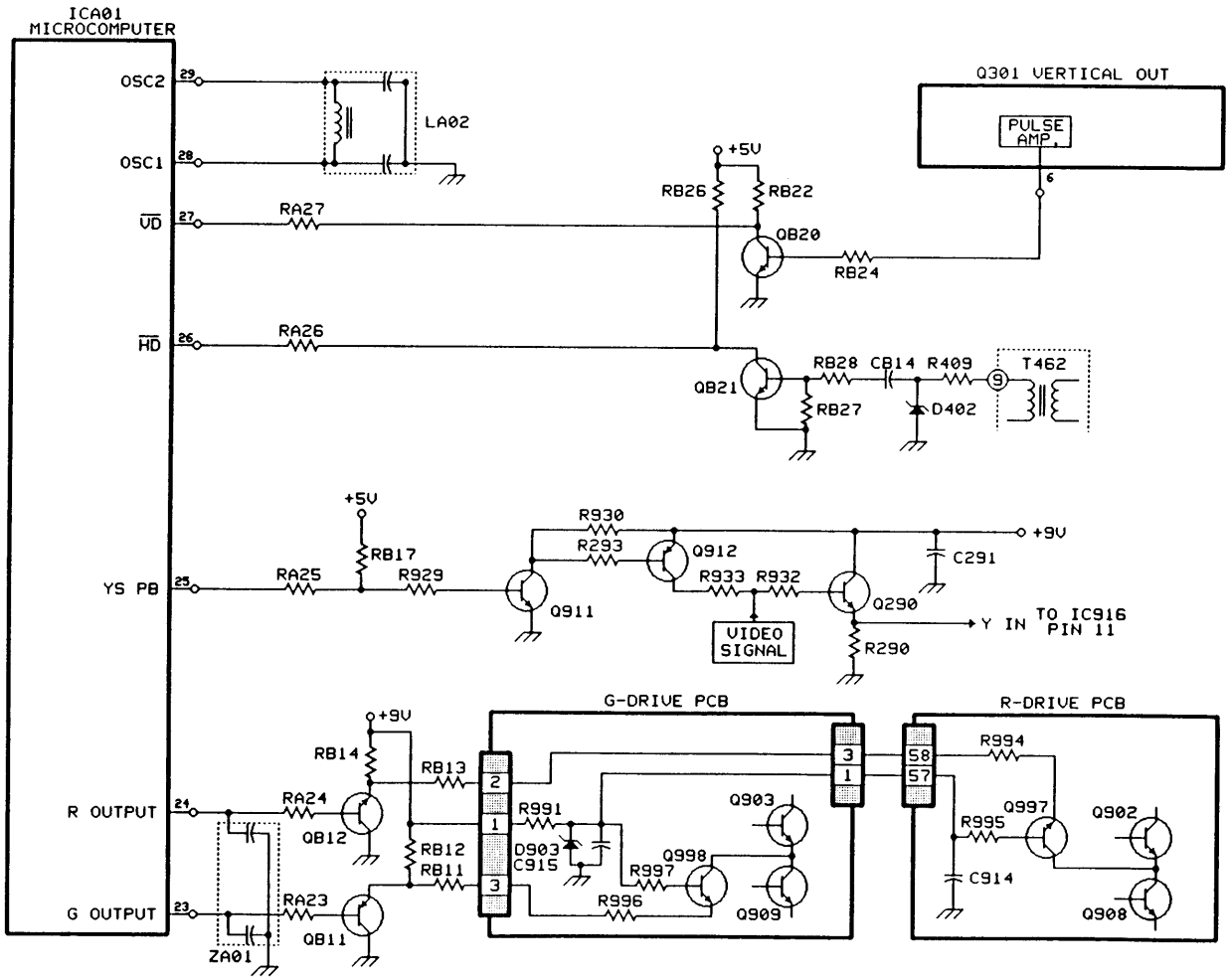


FIG. 8

NOTES

IV.

VIDEO/CHROMA PROCESSING

TUNER-PIF CIRCUIT OUTLINE

An RF signal induced on an antenna is converted into the intermediate frequencies of 45.75 MHz, for video and 41.25 MHz for audio within the tuner circuit. (Hereafter the intermediate frequency signals are called IF signals.) The IF signals are band-limited in passing through a SAW filter and are then detected by the PIF/SIF circuits, thus obtaining the video, audio, and AFT output.

Some of the major features in the tuner circuit includes;

1. The newly developed IC EL695LX1 (181CH) which includes a PLL circuit built within.

2. A wide band double surface acoustic wave filter (Z101) is used as the SAW filter.

3. A FS system is used for channel selection.

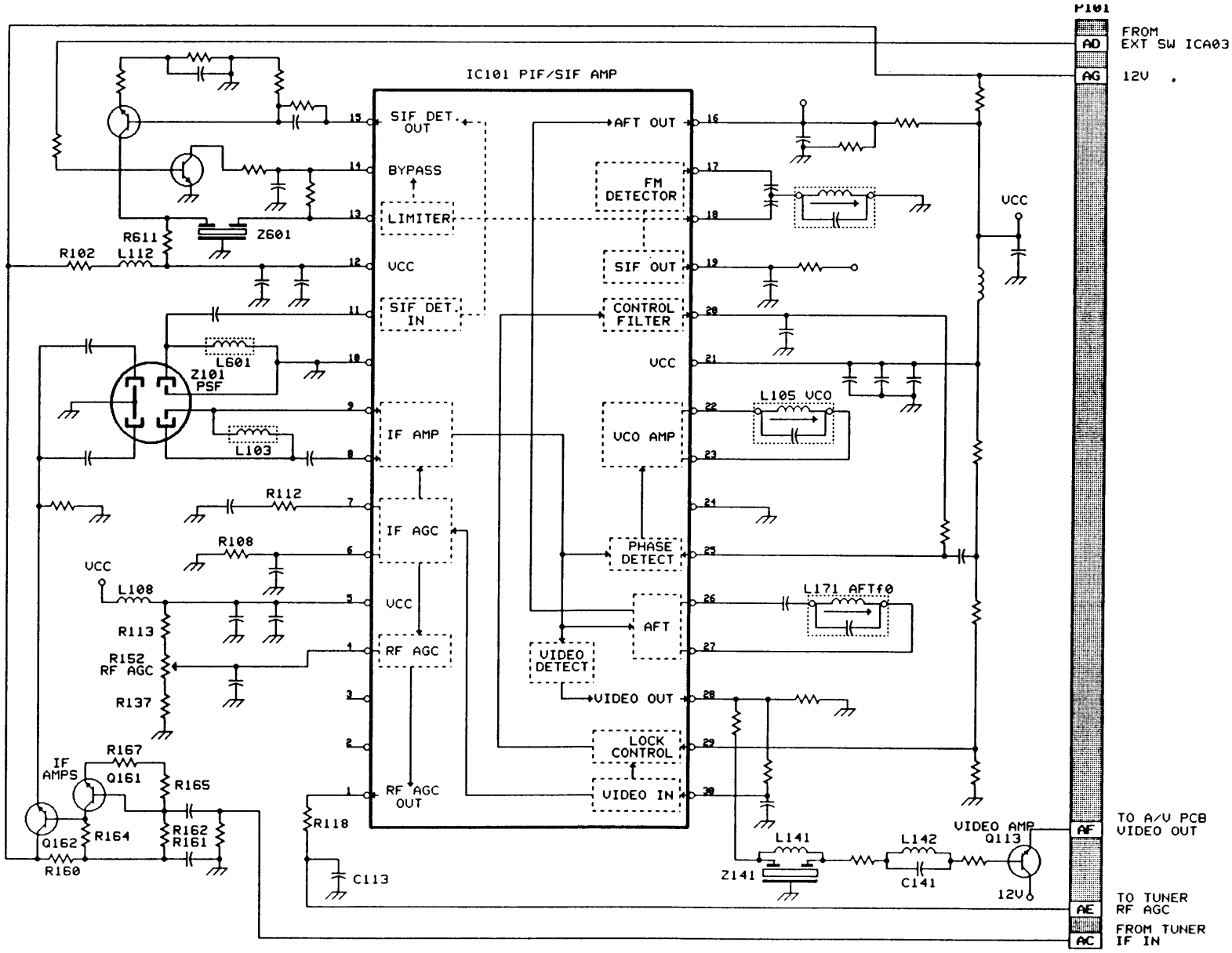
4. In the PIF/SIF circuits, PLL sync detection systems are employed, which results in the improvement of the following characteristics;

   A. Telop buzz due to video over modulation is eliminated.

   B. Improved reproduction characteristics of high frequency signal components are obtained.

   C. Cross color distortion and interference is eliminated.

PIF CIRCUIT


P101
AD
FROM EXT SW ICA03
AG
12V
IC101 PIF/SIF AMP
SIF DET. OUT
BYPASS
LIMITER
VCC
SIF DET. IN
IF AMP
IF AGC
VCC
RF AGC
RF AGC OUT
AFT OUT
FM DETECTOR
SIF OUT
CONTROL FILTER
VCC
VCO AMP
PHASE DETECT
AFT
VIDEO DETECT
VIDEO OUT
LOCK CONTROL
VIDEO IN
R611
Z601
R102
L112
L601
Z101 PSF
L103
R112
R108
VCC
L108
R113
R152 RF AGC
R137
IF AMPS
R167
Q161
R165
Q162
R164
R162
R161
R160
R118
C113
L105 VCO
L171 AFT f0
L141
Z141
L142
C141
VIDEO AMP Q113
12V
AF
TO A/V PCB VIDEO OUT
AE
TO TUNER RF AGC
AC
FROM TUNER IF IN

PIF CIRCUIT, AGC CIRCUIT

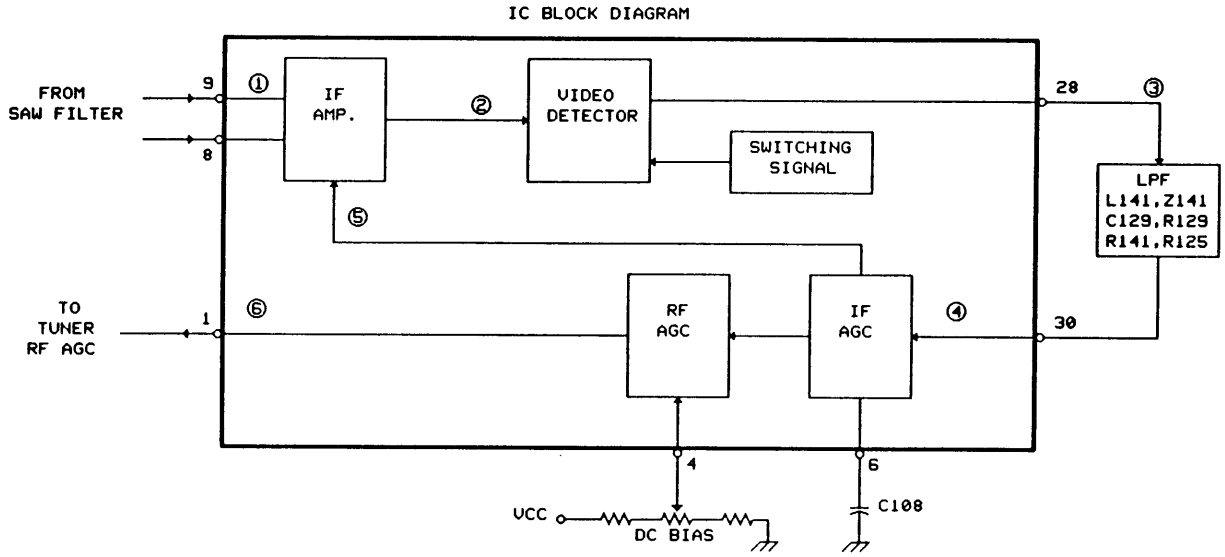
The PIF (Picture Intermediate Frequency) circuit amplifies and detects the IF signal from the SAW filter thus developing the video signal.

If a signal induced on the TV antenna varies in strength, the video detector output also varies. To prevent this, an AGC (Automatic Gain Control) circuit is provided to control the gain of the IF amplifier or the tuner, and thereby obtaining a constant output.

THEORY OF OPERATION

1. The IF signal corrected in its frequency response by the SAW filter is amplified at the IF Amplifier.
2. The amplified IF Signal is subject to multiplying detection with a Switching Signal (described in the PLL Circuit) to develop the video signal. Since phasing of the Switching Signal is -180 degrees from the IF Signal, the Video Signal is a negative sync type.
3. The video signal outputs the IC through pin 28.
4. The video signal is coupled through a LPF and then inputs the IF AGC circuit again with the harmonics eliminated.
5. The IF AGC circuit detects the sync tip voltage of the video signal fed back and thereby controls the gain of the IF amplifier. The IF AGC's time constant (response characteristic) is determined by C108 externally connected to pin 6 of IC101.
6. When the input field strength is high, the IF AGC circuit develops a control voltage for the RF AGC and varies AGC terminal voltage of the tuner, thus controlling gain of the amplifier inside the tuner. The field strength which starts operation of the RF AGC is determined by the DC bias supplied through pin 4 by R152 and applied to the RF AGC circuit. The RF amplifier is biased to operate at maximum gain. When the signal strength increases, the RF AGC voltage drops to decrease the gain of the RF amplifier (reverse RF AGC). The RF AGC voltage range is from +7V under weak signal conditions, to +1V for strong signal conditions. (Refer to RF AGC Delay adjustment.)

PIF/AGC CIRCUIT



PLL CIRCUIT

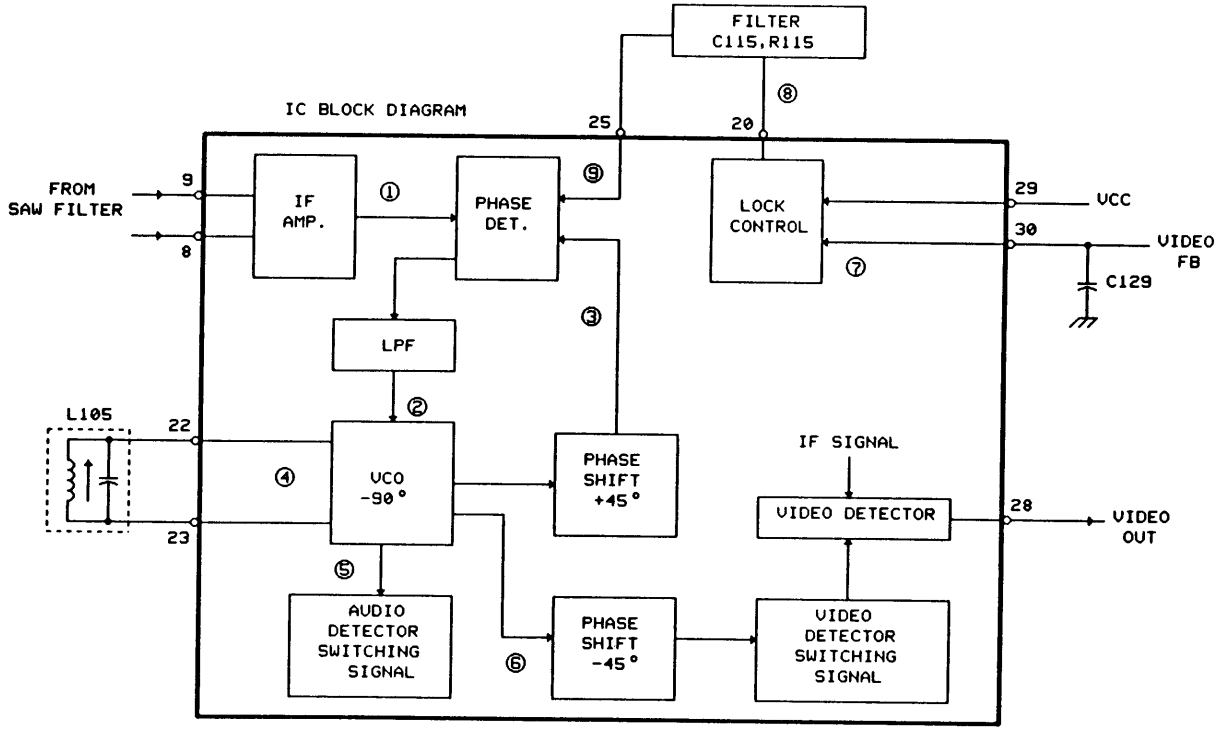
Detection operation is carried out incorporating a switching type detector to develop the Video and Audio Signals from the IF Signal. The PLL Circuit generates the Switching Signal.

In a conventional Quasi Sync Detection System, the Switching Signal is created by waveshaping the Video IF Signal. In the PLL Sync Detection System, the Switching Signal which has the same frequency as that of the Video IF Signal except for a specified phase difference is automatically generated.

THEORY OF OPERATION

1. The IF Signal is band-limited by the SAW Filter, amplified in IC101 and coupled to the Phase Detection Circuit.
2. A control voltage is applied to the VCO so that a phase difference of -90 degrees from the Video IF Signal is established.
3. The VCO output, (45.75MHz), passes through a +45 degree Phase Shift Circuit and again enters the Phase Detection Circuit. The VCO itself is locked at -135 degrees to the IF signal (-90 -45 = -135).
4. The reference frequency of the VCO is determined by adjusting the external coil L105. (VCO adjust.)
5. The Switching Signal for the audio signal detection is directly obtained from the VCO. (Phase difference of the switching signal the audio signal detection is -135 degrees to the video IF signal.)
6. On the other hand, the switching signal for video signal detection is also obtained from the VCO, but its phase is shifted an additional -45 degrees. (As a result, the phase difference of the switching signal for the Video Signal is -180 degrees to the Video IF Signal (-135 -45 = -180).
7. The video signal is coupled back to pin 30 of Q101 and smoothed by external capacitor C129 before entering the Lock Control Circuit.
8. Presence or absence of the video signal is identified by observing the DC voltage from pin 30.
9. If a video signal does not exist, the external filter (pins 20 & 25) is controlled so that the pull-in frequency range of the Phase Detection Circuit is increased to search for a video signal. In the same way, when the video signal exist, the filter is controlled so that the pull-in range is reduced to eliminate noise pick-up.

PLL CIRCUIT


IC BLOCK DIAGRAM
FILTER
C115,R115
⑧
25
20
FROM
SAW FILTER
9
8
IF
AMP.
①
PHASE
DET.
⑨
LOCK
CONTROL
29
VCC
30
VIDEO
FB
⑦
C129
③
LPF
②
L105
22
23
④
VCO
-90°
PHASE
SHIFT
+45°
IF SIGNAL
VIDEO DETECTOR
28
VIDEO
OUT
⑤
AUDIO
DETECTOR
SWITCHING
SIGNAL
⑥
PHASE
SHIFT
-45°
VIDEO
DETECTOR
SWITCHING
SIGNAL

VIDEO PROCESSING OVERVIEW

A composite video signal selected by the TV/Video Switching Circuit (ICV01) enters a CCD Comb Filter/ Vertical Edge Correction Circuit where the Y and C Signals are separated. The Y Signal is subject to black stretching and transmission rate correction in the Black Stretching Circuit, IC270. This processed Y Signal is then applied to pins 33 and 34 of IC501. Low and medium frequency components of the Video Signal input at pin 34, while pin 33 is the input terminal for high frequency components of the Video Signal.

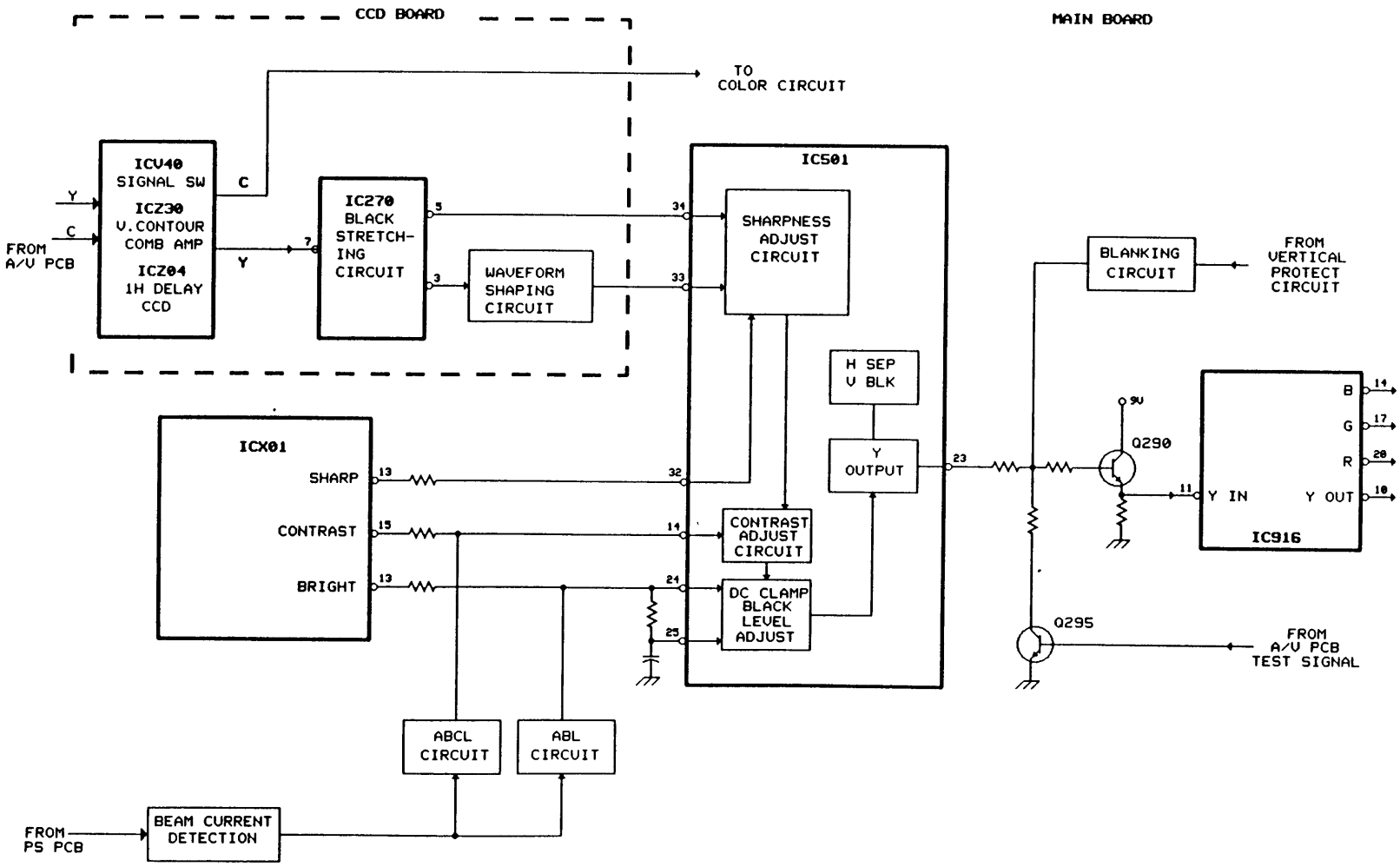
After entering IC501 the Video Signal is then added to a Sharpness Control Circuit and then fed to a Contrast Adjustment Circuit. A sharpness adjustment voltage from ICX01 and the addition of the low and high frequency components within IC501 varies the D.C. voltage set at pin 32, thereby adjusting the sharpness.

An established voltage from pin 15 of ICX01 is applied to pin 14 of IC501 to vary the gain of the contrast adjustment circuit. This circuit also uses additional controls from the ABCL and ABL Circuits. The D.C. voltage at pin 24 establishes the pedestal level. The DC voltage generated at pin 25 varies the clamp level set by pin 14 of ICX01, thereby adjusting the black level.

The output of the Contrast Adjustment Circuit, DC Clamp Circuit, and Black Level Adjustment are then coupled through the Y-output Circuit and outputs at pin 23. Blanking pulses are added inside IC501, and the output from pin 23 is coupled through emitter follower Q290 to the Matrix Output IC916 pin 11. The output of IC916 pin 11 is coupled to the Video Amplifiers Q270/Q276 and then applied to the G-DRIVE PCB. Here the signal will be dispersed between the G, B, and R-DRIVE PCBs.

The "Y" Signal input is also mixed inside IC916 with the R-Y, G-Y, and B-Y Signals that input pins 15, 18, and 21 to develop the proper Red, Green, and Blue Drive Signals.

VIDEO PROCESSING BLOCK DIAGRAM



VIDEO/AUDIO INPUT SWITCHING CIRCUIT

The Video/Audio Input Switching Circuits whose function is to switch the Video and Audio Signals of the antenna and external input signals (E1/S-VHS Video, E2 and Det. Output), consists of ICV01.

Each video input terminal provides one video input terminal and two audio terminals (L side is used as a mono jack) for each of the three available systems E1, E2, and S-VHS Video. If S-VHS Video is selected, then the audio terminals from E1 will automatically be selected as the audio input. Furthermore, the Y Portion of the S-Video Signal will enter ICV01 through pin 7 (same pin used by E1 Video Input).

A TV output terminal is also provided at the back of the unit.

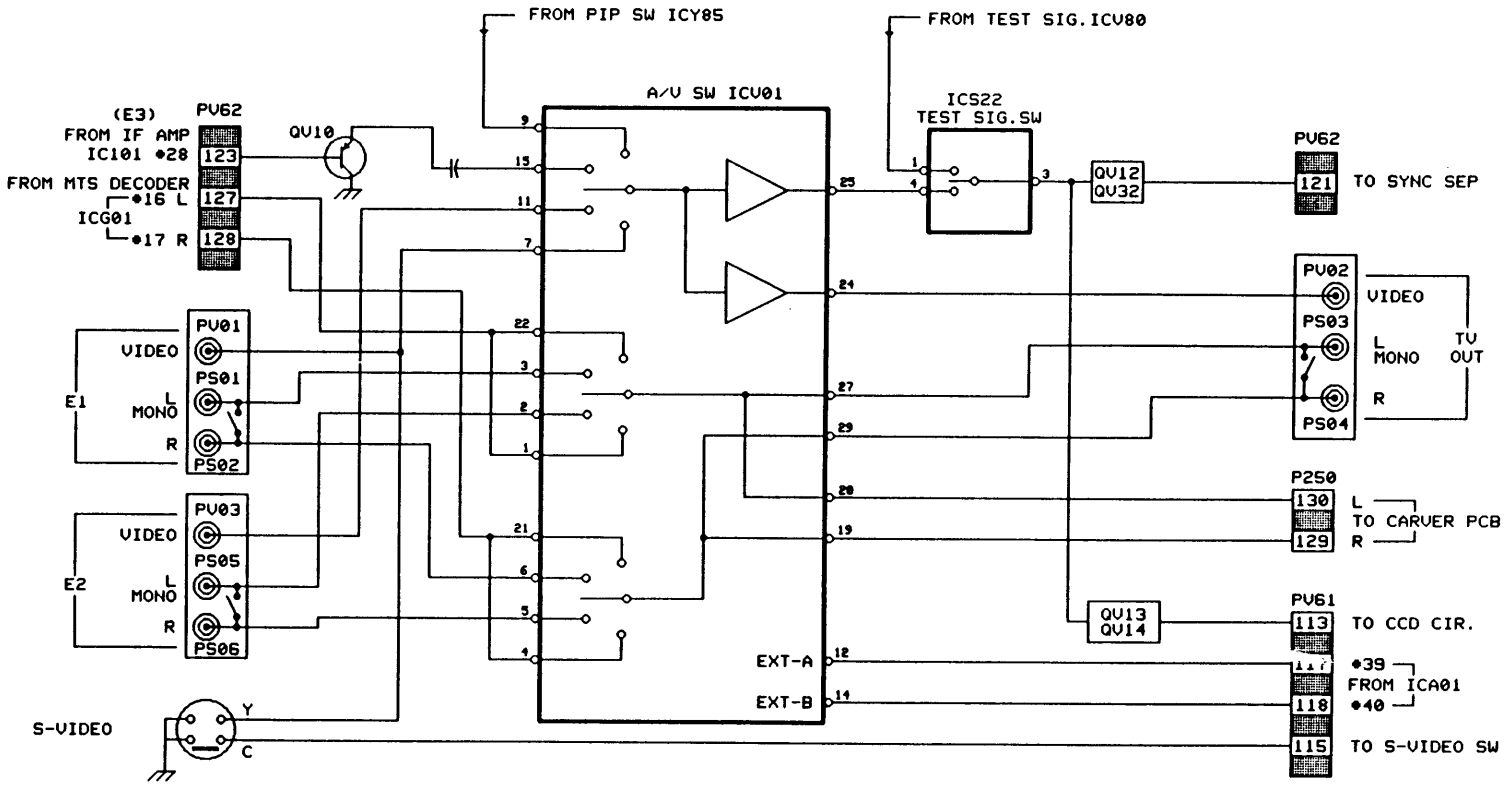
THEORY OF OPERATION

The detected TV Video from IC101 is coupled to the A/V Board and inputs the Switching ICV01 at pin 15. Each of the Video Signals (E1/S-VHS, and E2) inputs ICV01 at pins 7, and 11, respectfully. The TV Audio Signal (Lch, Rch) and each of the Audio Signals of E1/S-VHS,and E2 also inputs ICV01 at pins 1 through 6. The output at pin 25 is coupled to the CCD Circuit by passing through buffer QV12, a DC Clamp Circuit, amplifier QV13, and QV14 Buffer Circuit.

The Chroma Signal of the S-VHS Video is directly coupled to the S Video (S-VHS) Switching Circuit ICV40 on the CCD Board.

All selected audio signals from each system are coupled to the Audio Control Circuits.

A/V SWITCHING BLOCK DIAGRAM



CCD VERTICAL CONTOUR CORRECTION AND COMB FILTER CIRCUIT

The CCD Vertical Contour Correction Circuit consists of a 1H Delay and the associated circuits that perform vertical contour correction and Y/C separation. By using the CCD Circuit an increased frequency bandwidth of the video will be achieved. In addition, a clearer picture is obtained by combining the CCD with a concentrated electron beam CRT and a Wideband Video Output Circuit.

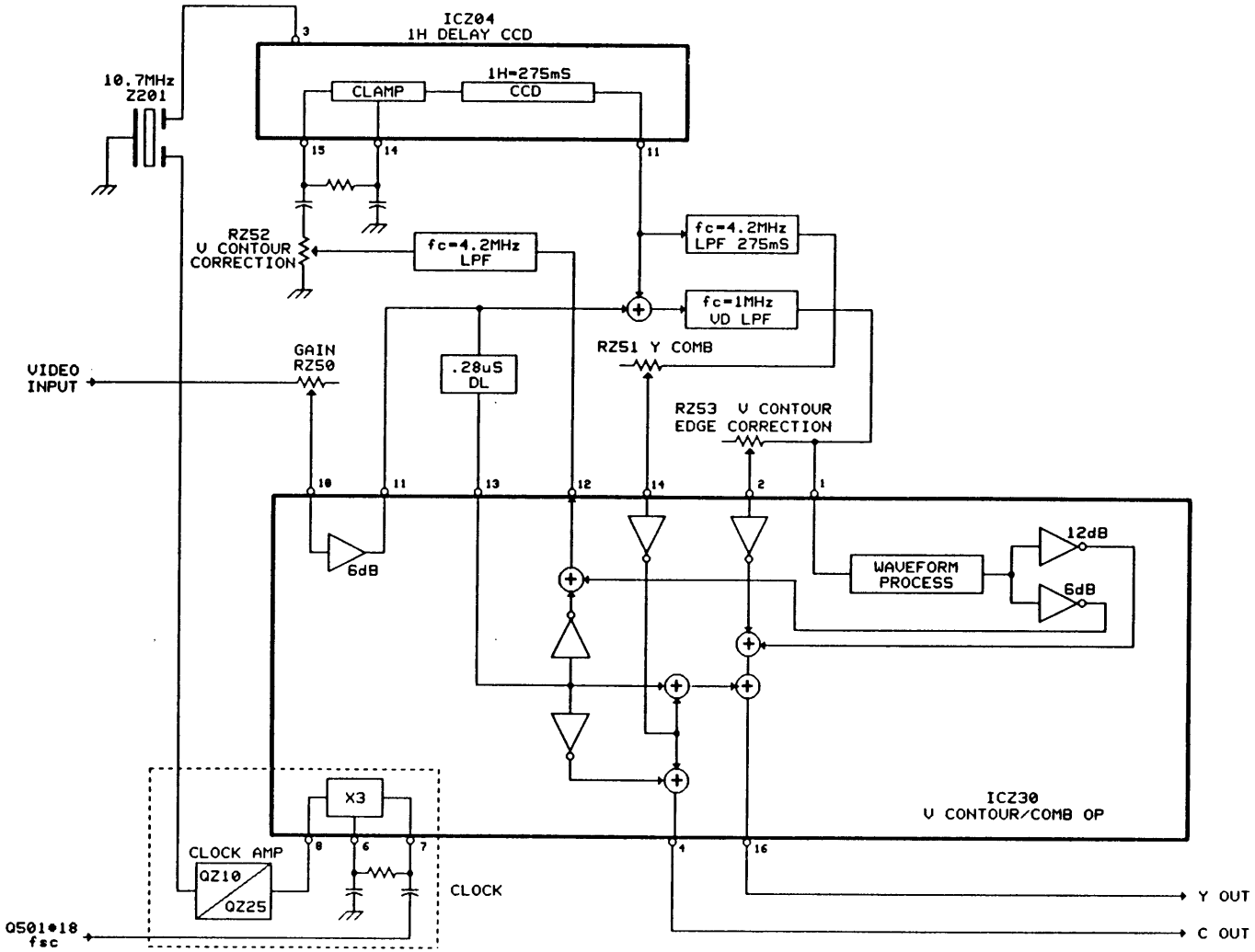
THEORY OF OPERATION

When the Composite Video Signal from QV14 on the A/V Input Switcher inputs pin 10 of ICZ30, it is increased by 6dB and outputs from pin 11. It then is split and one path is inductance coupled through a .28u sec. delay line XZ01. The signal inputs ICZ30 again at pin 13 where it is inverted and inputs ICZ04 pin 15 after being coupled through a LPF to eliminate harmonic distortion. After being delayed by 1H in the CCD Delay Circuit, the signal outputs at pin 11. It then is coupled through a 4.2 MHz LPF and inputs pin 14 of ICZ30.

The other signal path is added to the output of ICZ30 pin 11 for the filtering operation. This output is added to the signal that has been delayed by 1H, inverted and coupled through ICZ30. The added signals consist of the Edge Section, Color, and CCD Clock Components. The signal is then coupled through a VD Low Pass Filter (fc = 1MHz) to remove the undesired clock and color components. At this point the signal inputs ICZ30 at pin 2 where it is amplified and inverted. Within ICZ30, the developed signals are added together and are subjected to a waveshaping circuit for coring process, peak clip, and emphasis. At this time the Y and Chroma Signals are separated. Y outputs from pin 16 and the Color Signal from pin 4 of ICZ30 are DC coupled to pins 16 and 12 of the Signal SW ICV40.

The fsc (3.58 MHz) signal supplied from pin 18 of IC501 is capacitive coupled to pin 7 of ICZ30. Inside ICZ30 a tripler circuit converts the fsc signal into 3fsc to be used as the clock signal for the CCD.

CCD COMB FILTER & VERTICAL CONTOUR CORRECTION CIRCUIT



S-VHS VIDEO SWITCHING CIRCUIT

The S-video (S-VHS) Switching Circuit consists of ICV40. ICV40 toggles Luminance and Chroma Signal Systems preceding or following the CCD Comb Vertical Contour Correction Circuit. Since the S-video Signal already has the Y and Color Signal separated it is not necessary to use the CCD Comb/Vertical Contour Correction Circuit for signal separation.

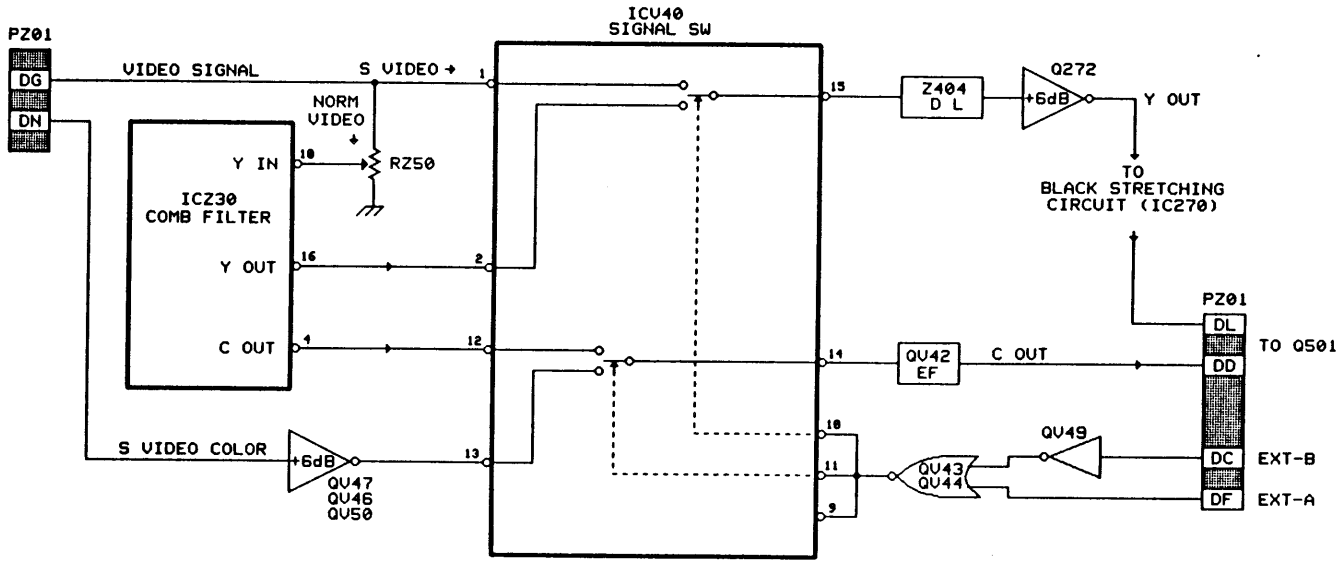
THEORY OF OPERATION

An EXT-A and EXT-B signal from microprocessor ICA01 inputs the CCD Board at DF and DC to be used as the S-video Switch Command. If the S-Video plug is conected to the back of the set, an internal switch (normally close to gnd.) will be pushed open and terminal DM (SW) at the CCD Board goes to high impedence (10V). Only when SW is at high impedence, the EXT-A is "L" and EXT-B is "H" will pins 9, 10, and 11 of ICV40 show "H" and place the IC in the S-video Mode. As a result, the incoming Y Signal enters pin 1 of ICV40 and is coupled directly to pin 15 of the same IC bypassing the CCD Comb Vertical Contour Circuit. From pin 15 the signal is coupled through the delay line XZ04 and 6dB amplifier Q272 and inputs the Black Stretching Circuit, IC270. At the same time, the S-color Signal entering the PC board at pin DN inputs ICV40 pin 13 after going through a 6dB amplifier circuit consisting of QV46, QV47, and QV50. Pin 13 is internally connected to pin 14, and the output S-color Signal is coupled through emitter follower QV42 to output the CCD Board at pin DD and input IC501 pin 31 on the Main Board.

When the EXT-A is not "L" and the EXT-B is not "H" (that is any combination other then), pins 9, 10, and 11 of ICV40 are set to "L" by NOR Circuit QV43 and QV44. In this, normal video condition, pins 2 and 12 of ICV40 are then connected to pins 15 and 14, respectively. The Y Signal from pin 15 is amplified about 6dB by Q272 and coupled through emitter follower Q271 to pin 7 of IC270 the Black Stretching IC.

The normal Chroma Signal at pin 14 is also coupled through emitter follower QV42, and follows the same signal path as the S-color Signal.

S-VHS SWITCHING BLOCK DIAGRAM



PICTURE SHARPNESS ADJUSTMENT CIRCUIT

The Picture Sharpness Adjustment Circuit will superimpose a secondary differential waveform on edge portions of the luminance signal. This sharpens the rising and falling characteristics of the edge portions by using preshoot and overshoot effects, thereby giving a clearer definition at the boundaries of pictures.

THEORY OF OPERATION

The input signal supplied from the CCD PC Board inputs the Main PC Board at terminal DL to the Sharpness Circuit. It is first differentiated by C202, R212, and L205, and then again differentiated by C207.

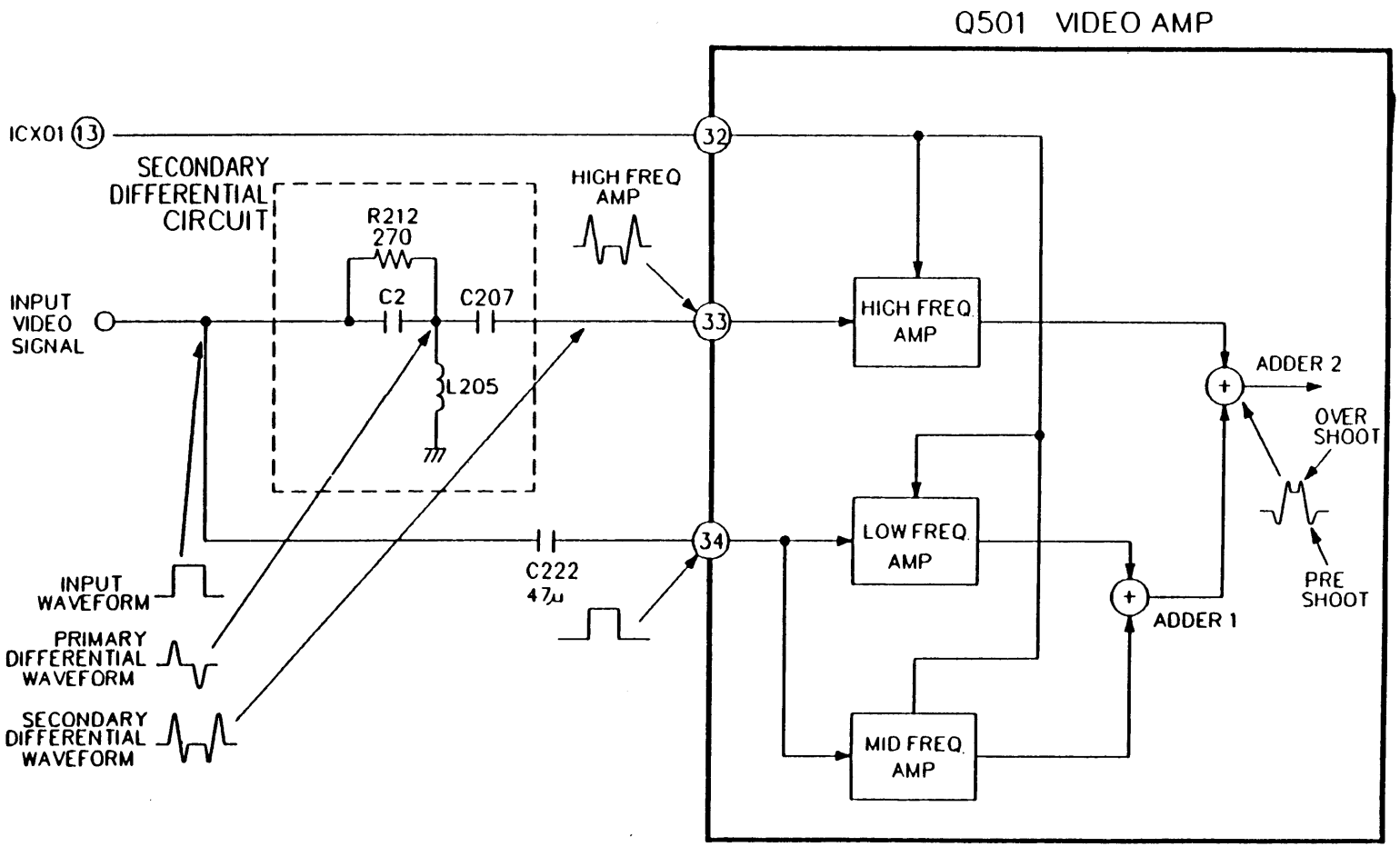
The differentiated signal inputs pin 33 of IC501 to the Picture Sharpness Circuit. Pin 33 provides for the input of the high frequency components of the video signal. At the same time, the video input is coupled through C222 to block the DC component. This signal also inputs pin 34, the terminal for the medium and low frequency components of the video signal. Within IC501, the input at pin 34 passes through a Low Range Amplifier and a Medium Range Amplifier and then is combined in the Adder #1 Circuit.

Now returning to the high frequency signal input at pin 33, observe that it is coupled through a High Frequency Amplifier and then is sent to Adder #2 where it combines with the product of Adder #1. At this time, the preshoot and overshoot effects are in operation to give improved contrast characteristics to the edge parts.

A DC Voltage from pin 13 of ICX01 is used as the picture sharpness adjustment control. This control voltage is applied to pin 32 of IC501 to vary the gain balance among the High, Medium, and Low Amplifiers to obtain an optimum frequency response.

The Processed Video Signal is now ready to enter the Contrast Adjustment and the Black Level Adjustment Circuits within IC501. After DC restoration and pedestal clamping, the Y Signal outputs IC501 at pin 23. Blanking pulses are added and this processed signal is coupled to the Y-output Amplifier Q290 and Matrix Control IC916. The Y Signal then will output the Main Board at connector 93 to be directly coupled to the CRT-DRIVE PC Boards.

PICTURE SHARPNESS ADJUSTMENT BLOCK DIAGRAM



BLACK STRETCHING CIRCUIT

The Black Stretching Circuit (located on the CCD PCB) is utilized in order to improve the contrast ratio by "stretching" the black most portion of the video signal to equal the pedestal level. It consists of IC270 and associated circuits.

The input signal from the Video Switching Circuit (emitter of Q271) enters at pin 7 of the Black Stretching IC. A sync signal developed at IC501, pin 28 (Video-Color IC) is waveshaped by Q275, C275, and Q274 and coupled to the input pin 3 of the Black Stretching IC. A blanking pulse (Horizontal and Vertical) is coupled through their respective OR Gates, D271 and D272 and is applied to IC270, pin 2.

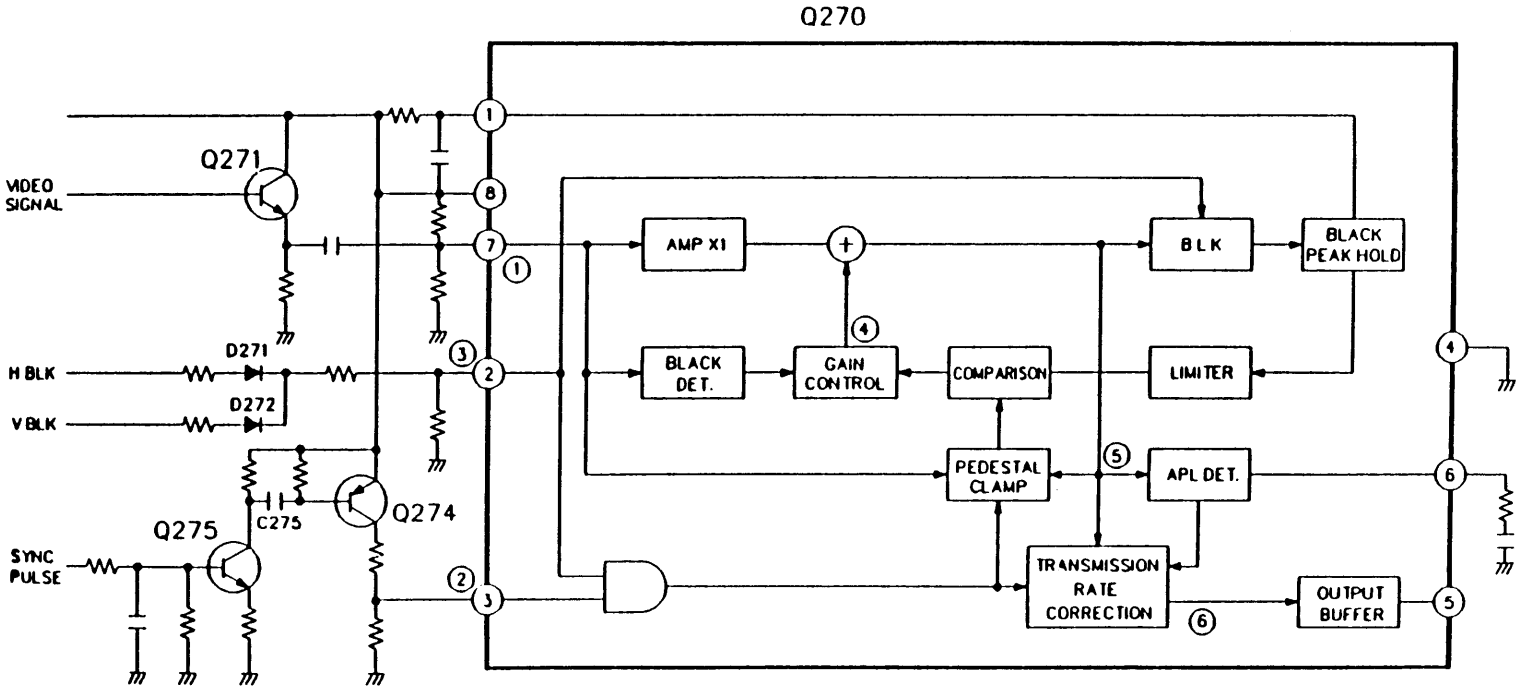
When a video signal enters the Black Stretching IC it passes through three types of circuits: Black Peak Hold, Black Detection, and Pedestal Clamp. Each of the outputs are compared and the difference voltage is used as a gain control. The gain control manages only the part of the video signal closes to the black level.

The Sync Pulse and H/V Blanking are used in the Transmission Rate Correction Circuit. This circuit maintains the proper control voltage to preserve the relationship between the Pedestal Level and the Average Picture Level (APL) of the video.

The results of these circuits in the Black Stretching IC insure that the black level is processed and clamped solid with respect to pedestal level for a clearer picture with vivid blacks.

The output of the Black Stretching Circuit at pin 5 of IC270 is then coupled to pins 33 and 34 of IC501.

BLACK STRETCHING CIRCUIT



AUTOMATIC CONTRAST ADJUSTMENT CIRCUIT (ABCL CIRCUIT)

To provide the picture with the desired contrast level, the Contrast Adjustment Circuit varies the AC level of the Video Signal and along with the ABCL Circuit will automatically reduce the contrast of a saturated Average Picture Level (APL) Signal to avoid deterioration in the linearity of black to gray response. In other words, improving the graduation quality of black tones.

THEORY OF OPERATION

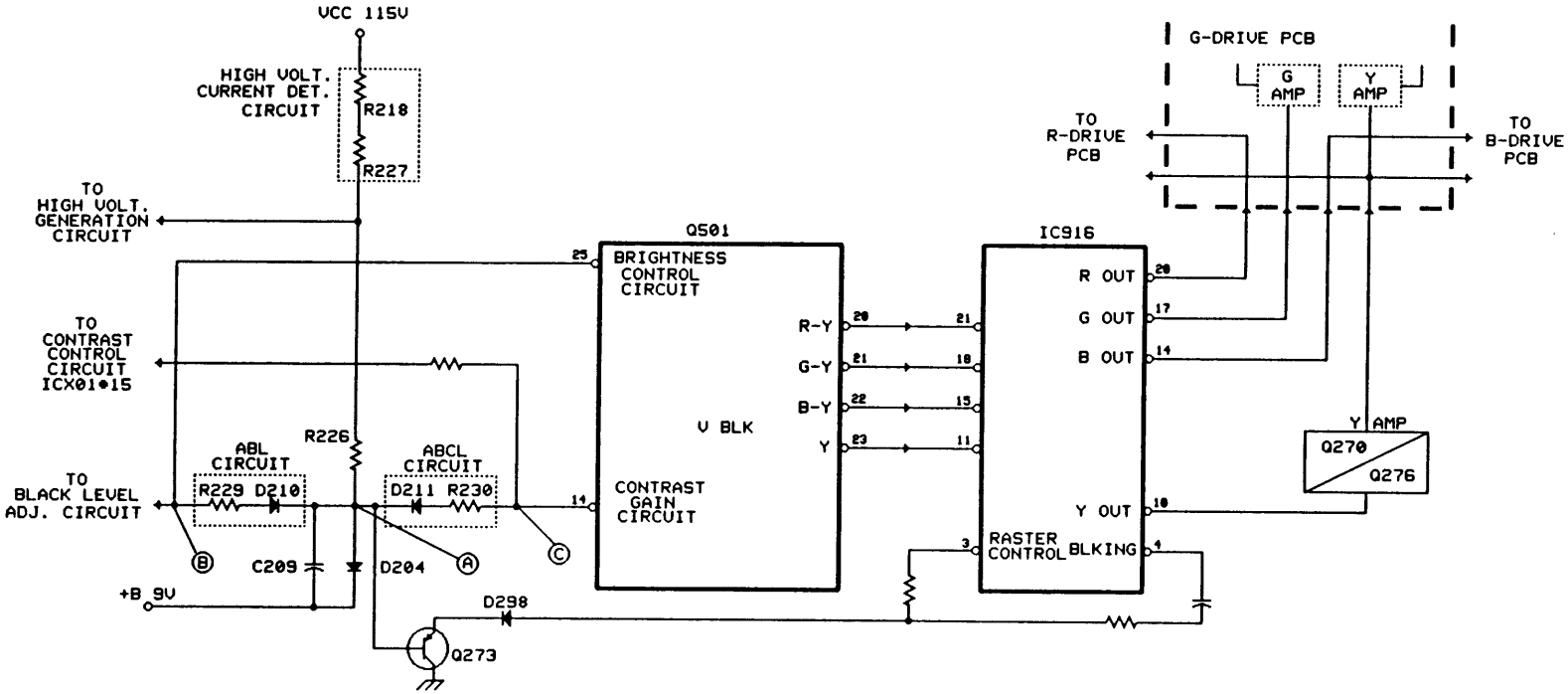
Referring to the figure below, R218 and R277 (located on the Power Supply PCB), detect current flowing into the anode of the picture tube. When the APL (Average Picture Level) increases, beam current increases and the voltage drop across R218 and R277 also increases. As a result, positive voltage at point A decreases and D210/D211 become forward biased.

With D210 conducting, the brightness control voltage at pin 25 of Q501 (point B) is clamped to the D.C. voltage at point A and the gain of the Black Level Adjustment Circuit is lowered thereby reducing the high voltage current. In this manner, the ABL Circuit protects the picture tube, flyback transformer, and the Horizontal Output Circuit by holding the high voltage below the maximum limitations of the beam current.

At the same time, when D211 conducts current flows into R230 and the voltage at point C lowers to less than 5V, thus decreasing the gain of the Contrast Circuit.

If the ABCL Circuit were removed and only the ABL Circuit existed, a high DC bias to decrease conduction of the CRT would be necessary to suppress the high voltage current that develops when a bright picture signal is present. This high DC bias, however, would lower the graduation quality of black tones. By using the ABCL Circuit to lower the AC gain of the video signal, a lower DC bias is needed to reduce the DC level of CRT conduction. The combined circuitry allows a constant brightness to contrast ratio impervious to changes in APL.

ABCL BLOCK DIAGRAM



BLACK LEVEL ADJUSTMENT CIRCUITS

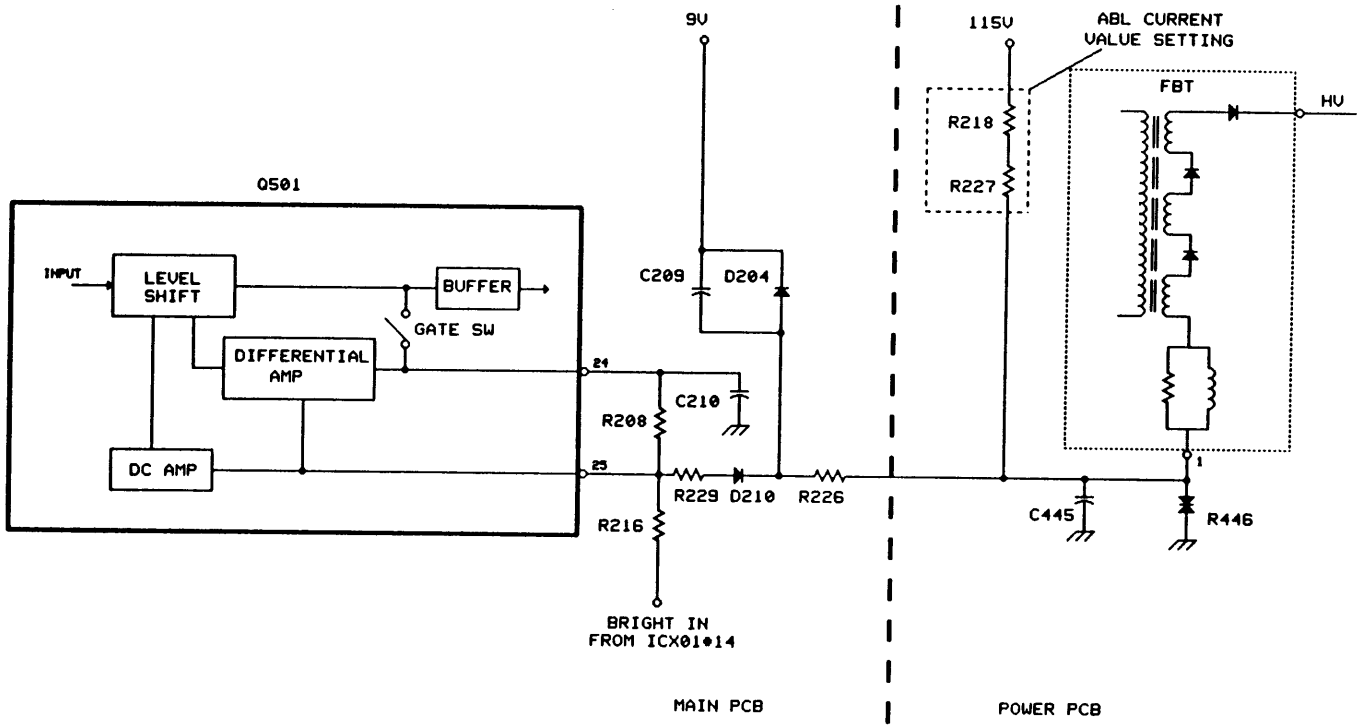
(Pedestal clamp, DC Restoration, ABL Circuit)

In TV receivers, the use of direct-coupled amplifiers are difficult because the gain from the detector output to the cathode of a picture tube is generally between 30 to 40dB, so capacitor coupled amplifiers are generally used.

In capacitive-coupled systems, the D.C. characteristics of capacitors cause pedestal level to vary with Average Picture Level (APL). As a result the black level also changes and this prevents precise reproduction of the signals broadcasted (DC restoration 0%). By suppressing the pedestal level variations due to the APL changes, the signal can be reproduced with 100% DC restoration and no brightness variations occur as the picture pattern changes. However, when the APL is low most of the video information exists near the black level, and when the APL is high most of the information exists near peak white. Since picture contrast differs considerably between the two cases, DC restoration is normally set between 70 and 90%. The DC restoration is managed after the pedestal level is clamped.

Additionally, to maintain the reliability of the picture tube, FBT, and horizontal output circuit, the ABL circuit limits picture brightness by detecting beam current.

BLACK LEVEL ADJUSTMENT BLOCK DIAGRAM



BLACK LEVEL ADJUSTMENT CIRCUIT (CONT.)

Theory of Operation

Pedestal Clamp Circuit

Pedestal clamping is necessary to maintain a stable black reference level. The pedestal clamp circuit is entirely contained within IC501. The video signals entering IC501 at pins 33 and 34 have a pedestal level that will vary with the APL. A differential amplifier is used in IC501 to insure that the pedestal level equals the difference between the black level voltage set by R216 and a DC voltage that corresponds to the pedestal level input at pin 25.

DC Restoration Circuit

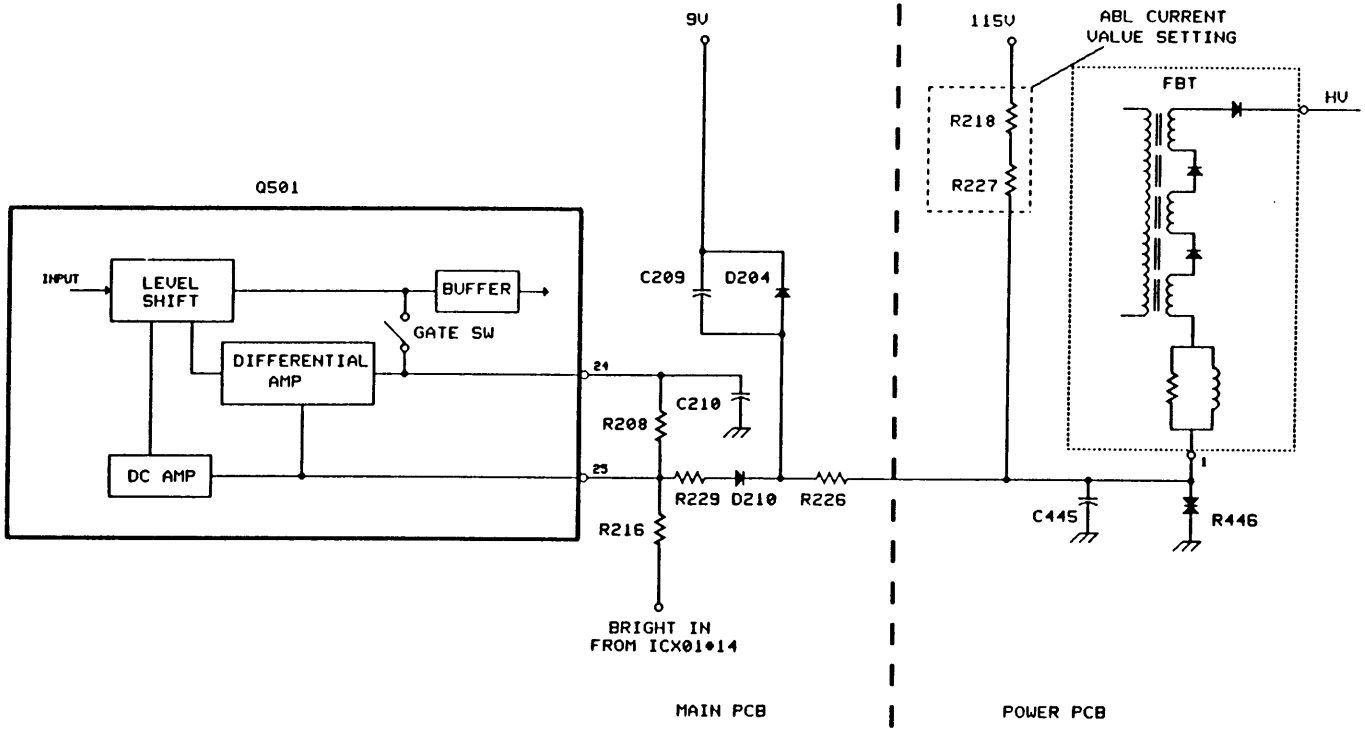
While DC restoration (clamping) is handled within IC501, the amount of restoration ratio can be determined by R208. If R208 was increased in value (open), the black level and pedestal level would remain the same regardless of APL. In other words, the pedestal level would be maintained at a constant level and a 100% DC restoration ratio is obtained. However, if R208 were to decrease in value (short), no pedestal correction would be carried out and the DC restoration ratio is 0%. Therefore, by selecting a particular resistance value for R208, the DC restoration ratio can be optimize.

ABL Circuit

ABL operation is carried out by D210/D204 and the high voltage current that flows from the 114V line through R218 and R277. Whenever the beam current is low along with a low Average Picture Level (APL), the voltage drop across R218/R277 is low. This causes the voltage at the cathode of D210 (at point D) to rise to a higher value and D210 turns off suspending ABL operation and allowing current to flow through the forward biased diode D204.

When beam current increases along with APL, the voltage drop across R218/R277 and at the cathode of D210 (point D) increases. D210 is now properly biased and turns ON while D204 turns off. The video signal is now biased towards less conduction and beam current is adjusted to a lower value.

BLACK LEVEL ADJUSTMENT BLOCK DIAGRAM



CHROMA SIGNAL PROCESSING

CHROMA AMPLIFIER

The color signal processing circuit is almost entirely contained whithin IC 501.

The circuits and functions inside IC501 include; Chroma Amplification, Chroma ACC (Automatic Color Control), APC, Hue Adjustment, Color Kill Detection, 3.58 MHz Oscillator, Burst Amplifier and Color Demodulation.

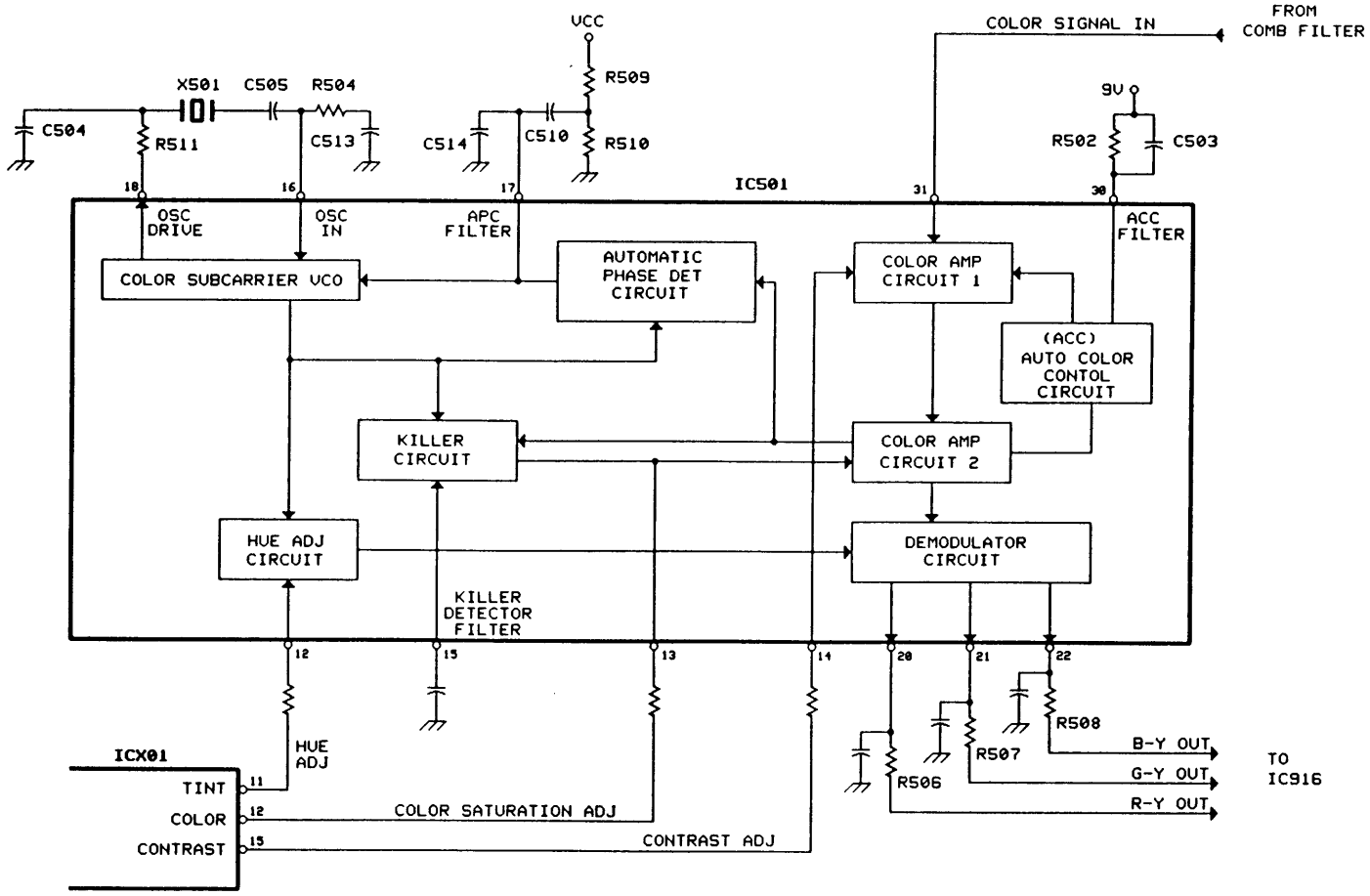
The selected Chroma Signal output of SW ICV40, is coupled through an emitter follower QV42 on the Comb Filter Board and inputs the Main PCB where it is coupled through a band-pass filter consisting of C501, C502 & L501, to pin 31 of IC501. The signal is amplified by the first and second chroma amplifiers, that are controlled by the ACC, Color Killer, APC, etc.

CHROMA ACC

ACC is accomplished by sampling the amplitude of the burst pulse at the output of the 2nd Chroma Amp. Circuit discription is as follows;

The Burst Signal is rectified into a DC voltage by the ACC Circuit and is used to control the gain of the first Chroma Amplifier. C503 & R502 connected to pin 30 serve as a filter for the DC voltage and keep the ACC voltage being applied to the First Chroma Amplifier constant and not subject to noise or instantaneous signal fluctuations.

CHROMA PROCESSING IC



3.58 MHz OSCILLATOR & A.P.C.

The 3.58 MHz Sub Carrier Re-insertion Signal is necessary to demodulate the Red, Green and Blue Chroma Signals applied to the Demodulator Circuit. Simple phase demodulation occurs at the Chroma Demodulator.

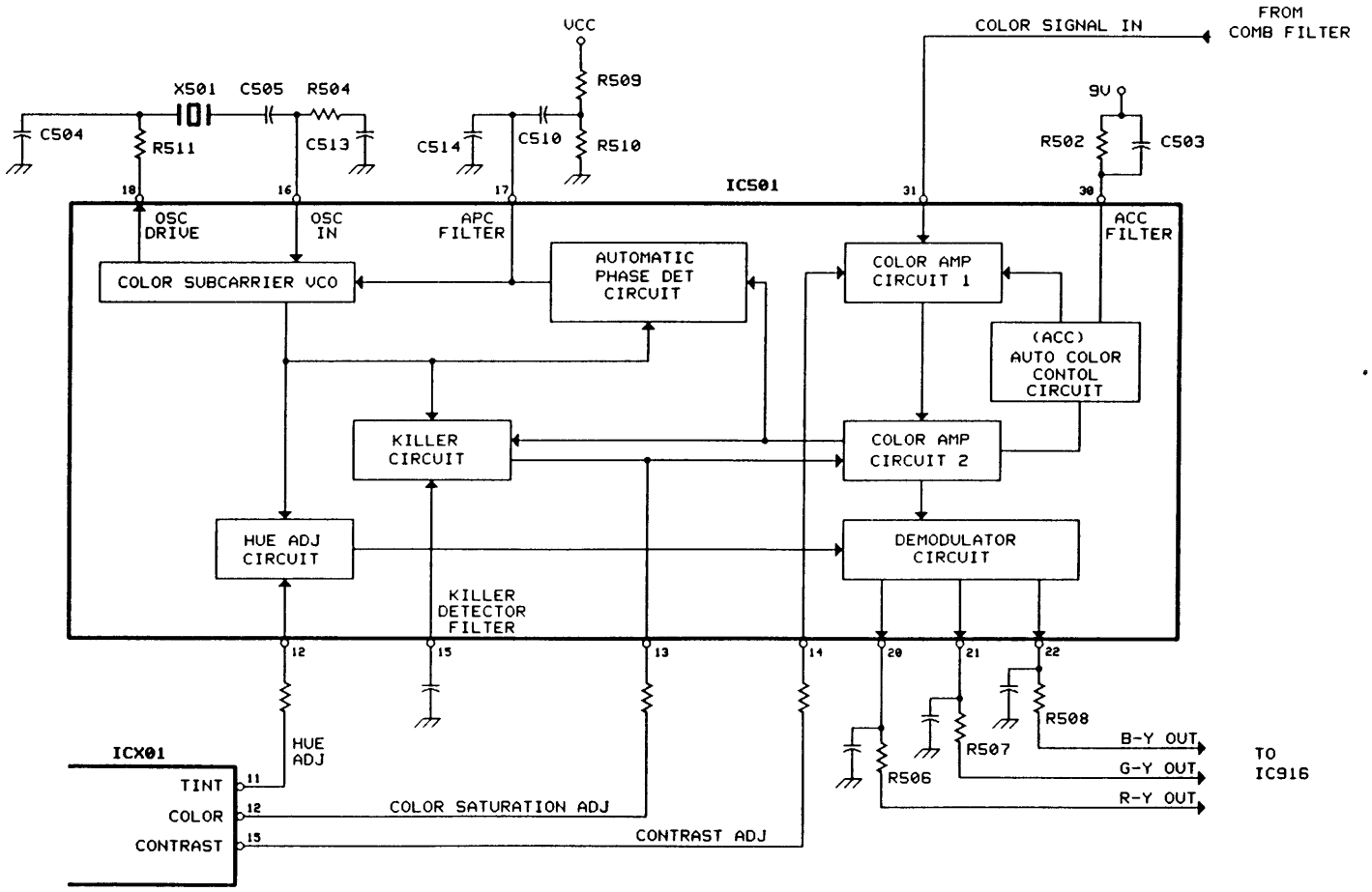
In order to reconstruct the original chroma signal broadcast, it is necessary to phase lock the 3.58MHz oscillator signal generated in IC501 to the phase of the incoming Burst Signal. This is accomplished by sampling the burst signal from the Second Chroma Amplifier and phase comparing it to the output of the Color Sub Carrier VCO. Any phase difference develops a DC correction voltage which is applied to the Color Sub Carrier VCO. The main frequency determining components of the 3.58MHz Oscillator are R511, C504, R504, C513, X501 and C505

The phase locked 3.58 MHz Oscillator Signal is then applied through a Hue Adjustment Circuit and finally to the Demodulator Circuit.

HUE ADJUSTMENT CIRCUIT

A variable D.C. voltage at pin 12, established by ICX01, causes the phase of the 3.58 MHz Reinsertion Sub Carrier to be shifted. To perform hue correction, the Sub Tint Control connected to pin 12 of IC501 adjusts the preset phasing of the Hue Control Circuit.

CHROMA PROCESSING IC



DEMODULATOR

The demodulator compares the phase of the incoming Chroma Signal from the Second Chroma Amplifier to the phase of the 3.58 MHz Sub Carrier Signal. The resulting output at pins 20, 21 & 22 of IC501 are the reconstructed R-Y, G-Y and B-Y Chroma Signals.

These signals are directly coupled to the Matrix output IC916 pins 15, 18, and 21. Here the chroma signals mix with the Luminance Signal applied at pin 11 thus developing the Red, Green and Blue Drive Signals applied to the CRT cathodes.

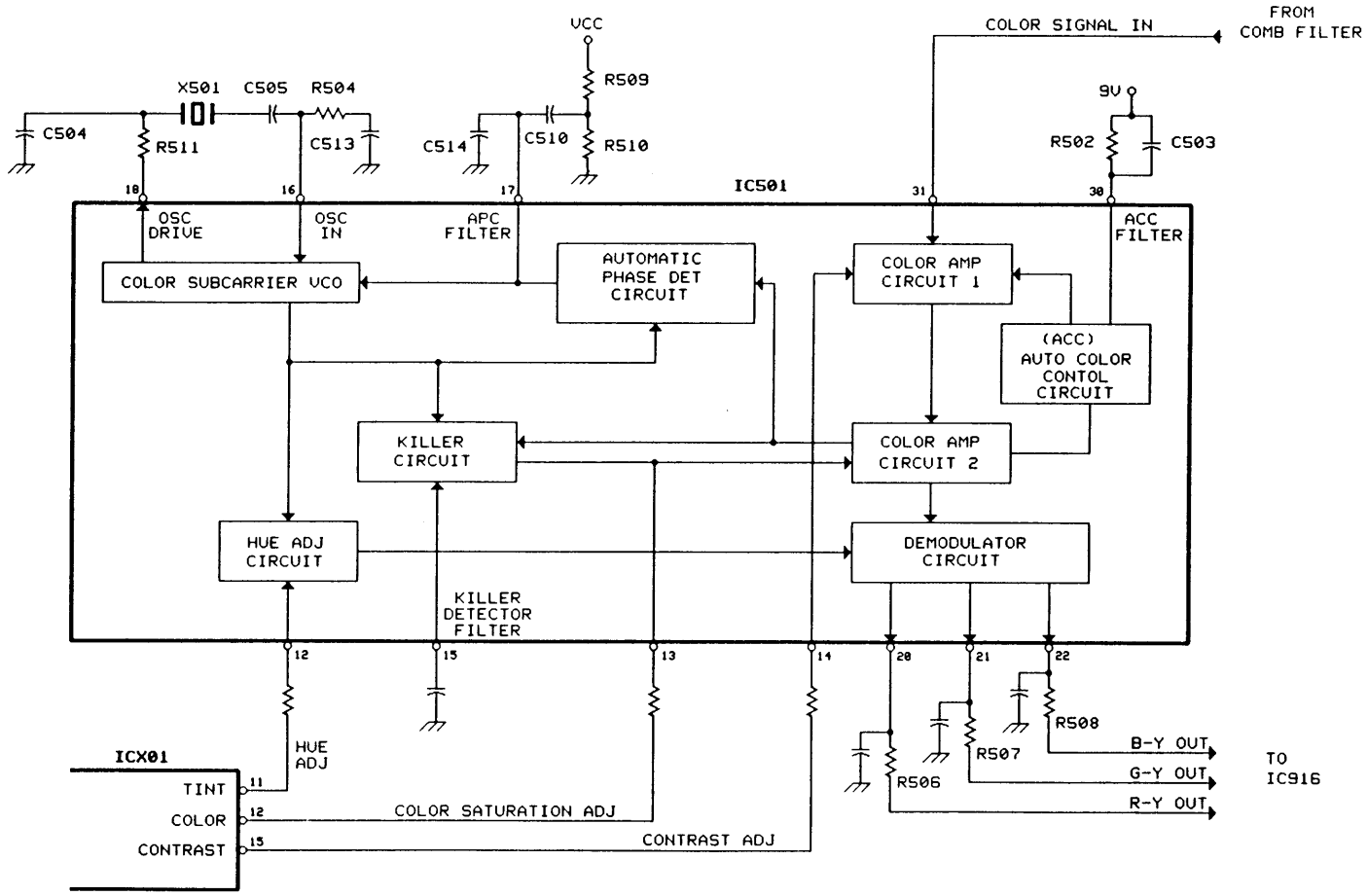
COLOR KILLER

The Color Killer Detector Circuit functions to turn "OFF' the Second Chroma Amplifier during a B/W broadcast by detecting the presence or absence of burst present at the Second Chroma Amplifier.

During a color broadcast, the Color Killer detects the presence of burst present at the Second Chroma Amplifier. The Color Killer is turned "OFF" which causes the voltage at pin 15 to go high, or approximately 9 volts.

When a B/W program is received, there is no burst signal present at the Second Chroma Amp. The Color Killer detects this and turns "ON" to turn "OFF" the Second Chroma Amp. With the Color Killer "ON", the voltage at pin 15 drops to about 5.5 volts.

CHROMA PROCESSING IC



NOTES

V.

PICTURE IN PICTURE

PIP (SUB-PICTURE) SYSTEM

Toshiba's Picture-in-Picture has greater versatility then ever before. PIP features include:

SIZE: The PIP can be changed from 1/4 to 1/16
SWAP: The main picture and PIP picture can be exchanged.
STILL: The PIP picture can be frozen.
CHANNEL SEARCH: A PIP picture of four channels in sequence will appear at the bottom of the screen.
POSITION CHANGE: The PIP picture can appear in any corner of the screen.
SEQUENTIAL SEARCH: Four frames will advance with a progression of still frame images.

The PIP System is contained on the PIP Board UX01. This circuit will change Sub-picture Video Signals into Analog RGB Signals. This signal is then inserted into the main picture. The block diagram of the PIP System is shown in Fig. 1.

Here the PIP system is described by dividing it into the following 4 sections:

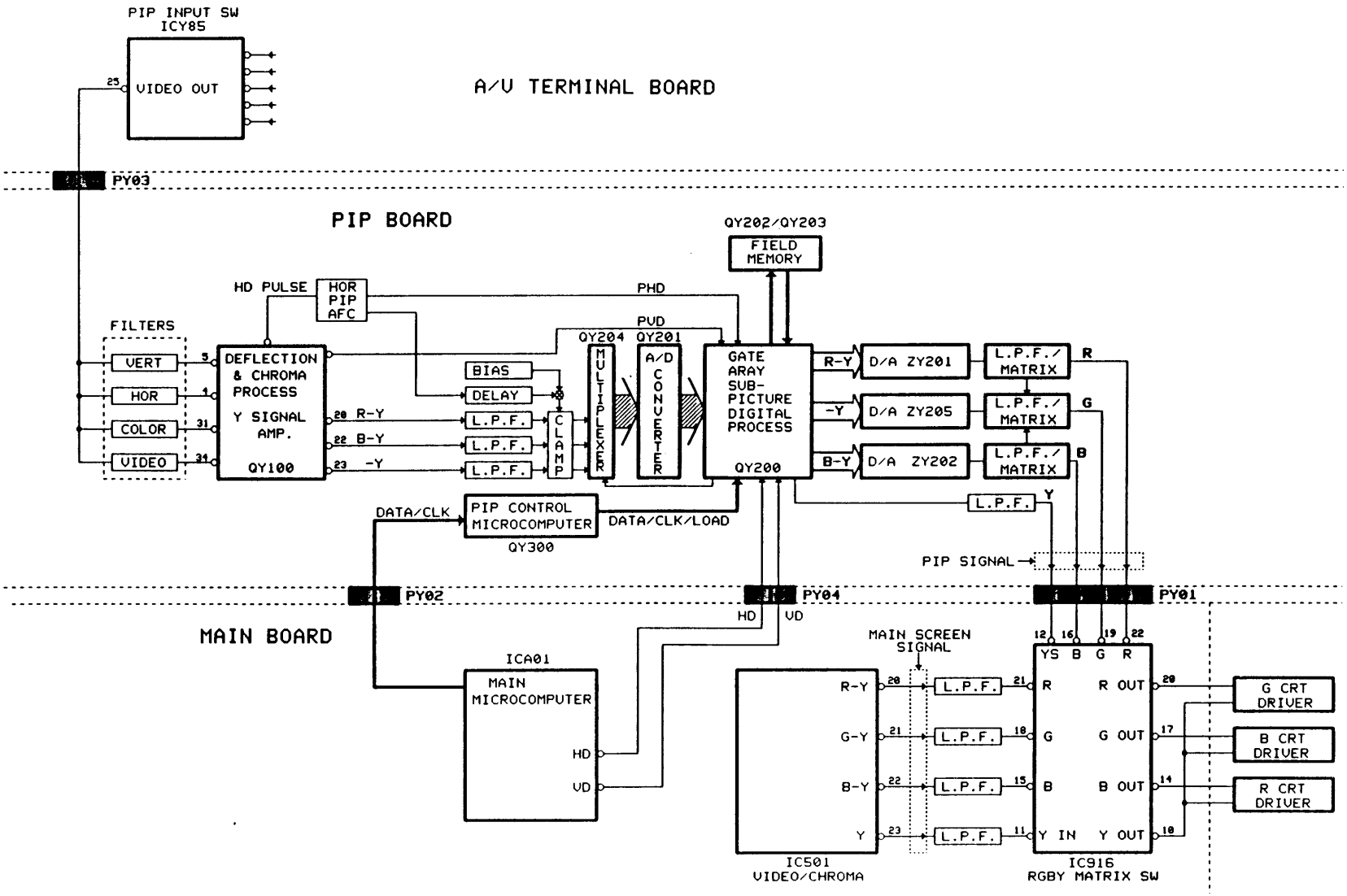
I. Circuits involved in video/chroma processing of the input video signals.

II. Circuits involved in digital processing of converted digital signals for analog conversion.

III. Circuits involved in output of luminance and color difference signals as RGB signals.

IV. Microcomputer interface circuit for operating digital circuits.

PIP SYSTEM BLOCK DIAGRAM



PIP CIRCUIT (Cont.)

VIDEO/CHROMA PROCESSING UNIT

This Sub-picture System consist of a circuit that converts video signals into the Luminance Signal (Y) and Color Difference Signals (R-Y, B-Y), and inserts them into the Main Picture. In this section the Video/Chroma Processing Circuit of the PIP system is described along with signal flow. Refer to Fig. 1 which shows the block diagram of the PIP system and the RGB Circuit.

THEORY OF OPERATION

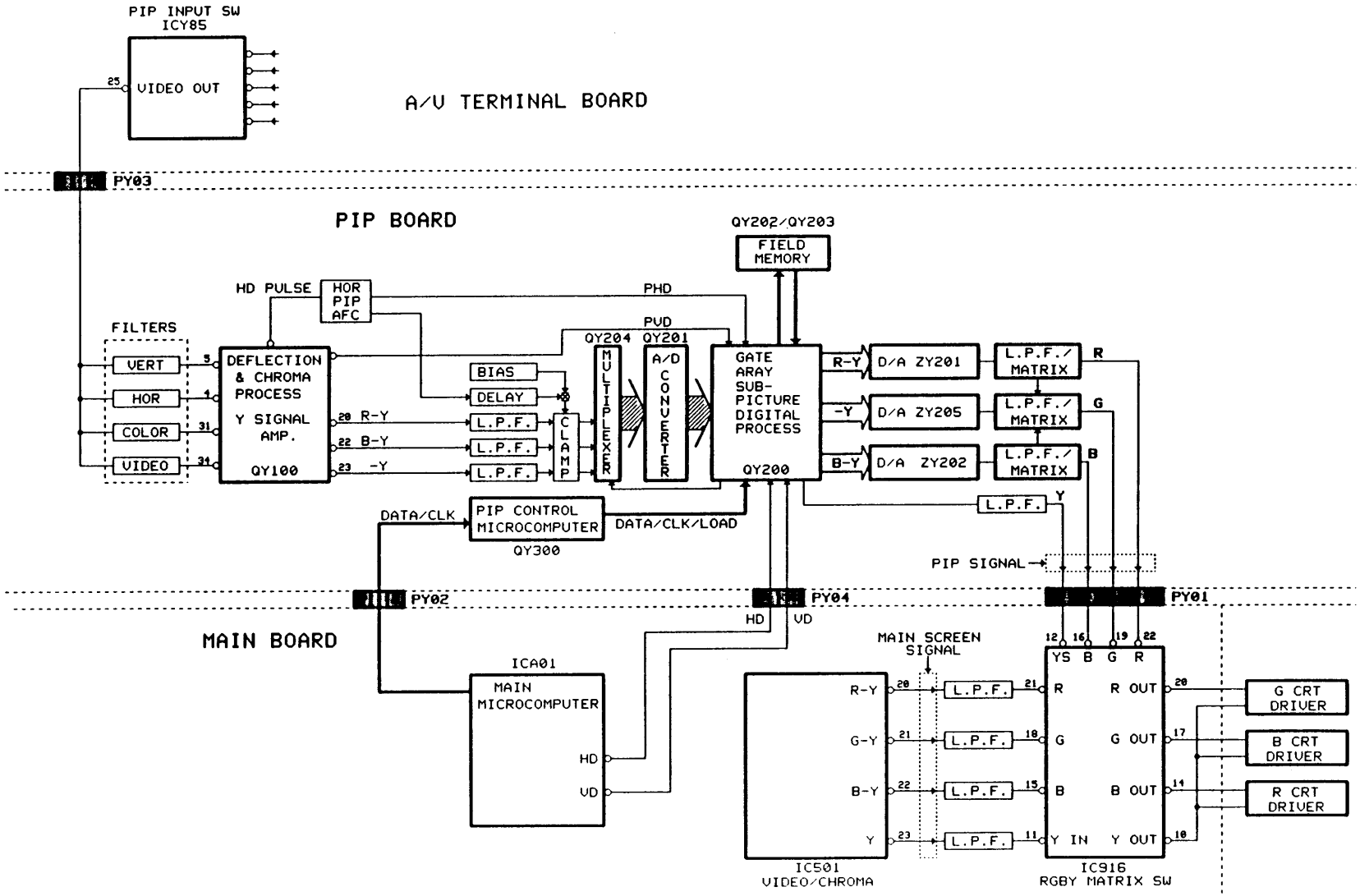
Video/Chroma Processing

QY11 performs Video/Chroma processing, PIP Video Signal contol, and V/H psuedo sync processing. The Video Signal Output from the Sub-picture AV Switching Circuit, inputs to pins 33 & 34 of QY100, after removal of the color signal components. The color signal inputs the IC through pin 31. RY103 and CY100 make up an integration circuit used for Vertical Sync separation at pin 5. RY100 and CY101 make up an integration circuit used for horizontal sync separation at pin 4. Contrast, Hue, Shade and Brightness are also regulated in the Video Chroma Circuit. The Y Signal is output at pin 23, while R-Y and B-Y Signals are output from pin 20 and 22 respectively.

Sub-picture Sync Signal Generating Circuit

The Sub-picture Sync Signal Generating Circuit is concentrated around the Video/Chroma IC QY100. A Sub-picture Vertical Sync Signal (PVD) is produced by shaping the output signal from pin 36 of QY100 by Vertical Driver QY103. The Sub-picture Horizontal Sync Signal (PHD) is developed at the Horizontal AFC Circuit by using pseudo-flyback pulses as a stabilized sync signal. When the switching transistor QY102 is turned ON by the horizontal drive pulses (HD) that output pin 10 of QY100, a pseudo-flyback pulse is developed through the resonance of CY131 and LY104. The flyback pulses are integrated by RY148 and CY134 and the resulting sawtooth pulses obtained input pin 6 of QY100. This way a stable AFC sawtooth operation is performed. The PHD signal finally outputs after passing through the wave shaping transistor QY104.

VIDEO/CHROMA PROCESSOR



PIP (SUB-PICTURE) SYSTEM (Cont)

In this system the circuit digitally converts Y Color Differential Signals and displays them as pictures in reduced size (sub-picture display).

Pin names and functions of the Gate Array are shown in Table One.

THEORY OF OPERATION

A/D Converter

The -Y, R-Y and B-Y Signals which are supplied from the Video/Chroma Processing IC are pre-processed in this circuit before being input to the A/D Converter QY201, (See Fig. 2). All three input signals are coupled through a Low-pass Filter Block where band limiting is performed. The value of the low-pass filters are 1.3MHz for -Y and .5MHz for the R-Y/B-Y signals. Band limiting is done to prevent the generation of "Conversion Noise" (Fold over Noise) which occurs at the time of A/D conversion. The pre-processed signals are then applied to a Clamp Circuit which consist of transistors QY205 through QY213.

In the Clamp Circuit the pedestal level is set so that the input signals are clamped accurately to the input range of A/D Converter (1v p-p max.). Clamped signals are then coupled through the Multiplexer (MPX) QY204 and inputs through pin 12 of the A/D Converter as Time Sharing Data. Shown in Fig. 3 is the concept of this MPX. The data is input to the A/D Converter at regular intervals of; -Y, -(R-Y), -Y, -(B-Y), -Y and -(R-Y) signals, and so on.

The A/D Converter IC takes the input analog signal and converts it into a 6-bit PCM Signal. The Clock Frequency (pin 7) is 5.4 MHz, and is coupled from pin 96 of the PIP Processor IC. An external bias circuit supplies IC QY201 with the input comparison voltages of 5V at pin 11(VRT) and 4V at pin 13(VRB). This gives the IC a 1 volt input range which is divided into 63 steps. This processed signal outputs as 6-bit data. These output signals (D1->D6), are now coupled to the PIP Processor IC.

A/D CONVERTER & MPX CONCEPT

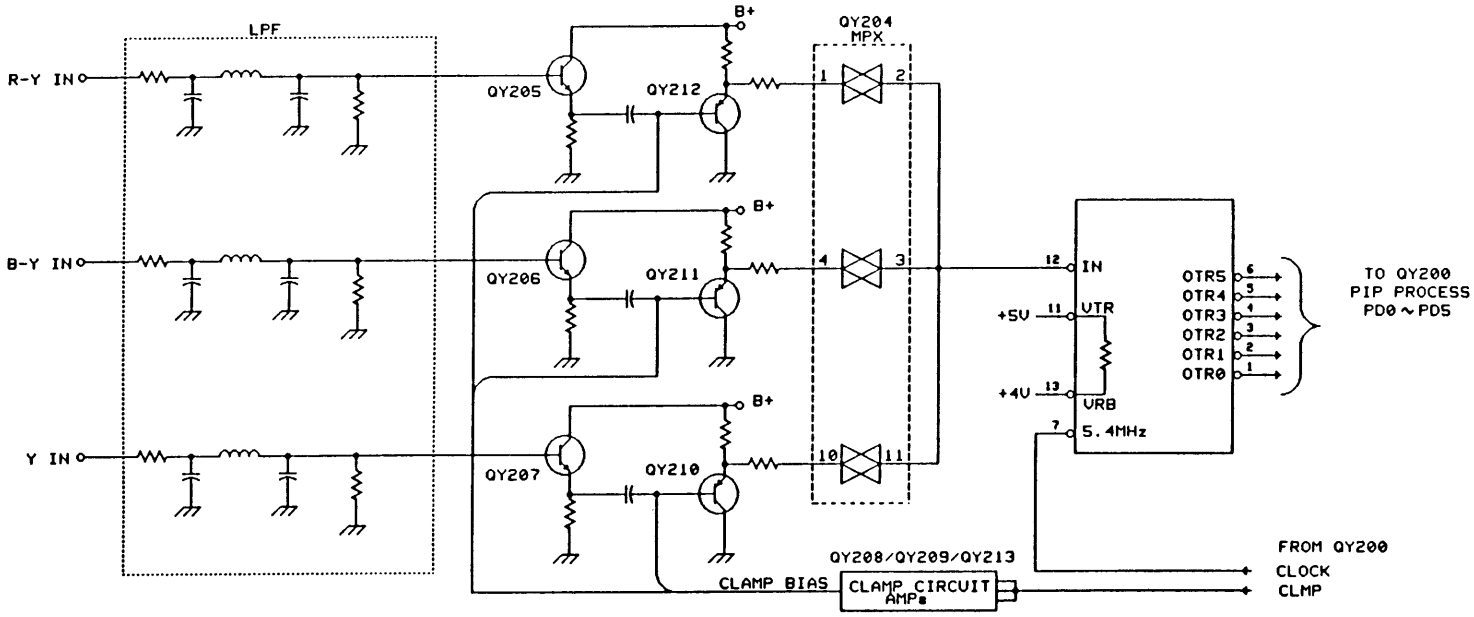


FIG. 2

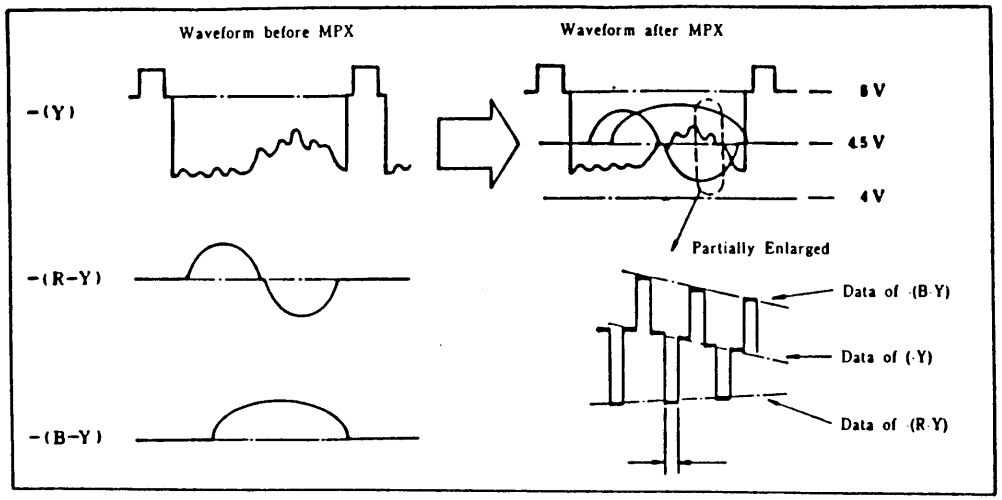


FIG. 3

THEORY OF OPERATION

Figs. 4 and 5 show the quantity of data written on the sub-picture and quantity of data displayed on the main picture. Fig. 4(a) shows that sub-picture video (Y) is written into memory as 260H/Field. One field of memory out of each frame of the sub-picture video data is useful data for processing. Fig. 4(b) and (c) show the state where the sub-picture is displayed synchronously with the main picture.

In the case of Fig. 4(b), the circuit is using 260H/Frame and thereby will display 130H/Field (1/4 Picture Size Display); 1(1), 1(3), 1(5) and so on are displayed in the odd field of the main picture and 1(2), 1(4), 1(6) and so on are displayed in the even field of the main picture.

In the case of Fig. 4(c), the circuit is using 130H/Frame and thereby will display 65H/Field (1/16 Picture Size Display) data is read and displayed from memory by skipping over 1 line in both the horizontal and vertical directions. So that 1(1), 1(5), 1(9) and so on are displayed in the odd fields and 1(3), 1(7), 1(11) and so on are displayed in the even fields.

Fig. 5 shows the state of the write/read video data in the multi-mode. Fig. 5(a) shows that video data for the sub-picture is written as 130H/Frame, same as 1/16 Picture Size Display. In this mode, video from one field of each frame is useful data. Fig. 5(b) shows that the sub-picture is read and displayed at 65H/Field according to the odd fields and the even fields of the 1/16 Size Picture.

WRITE/READ OF 2 & MULTI VIDEO DATA

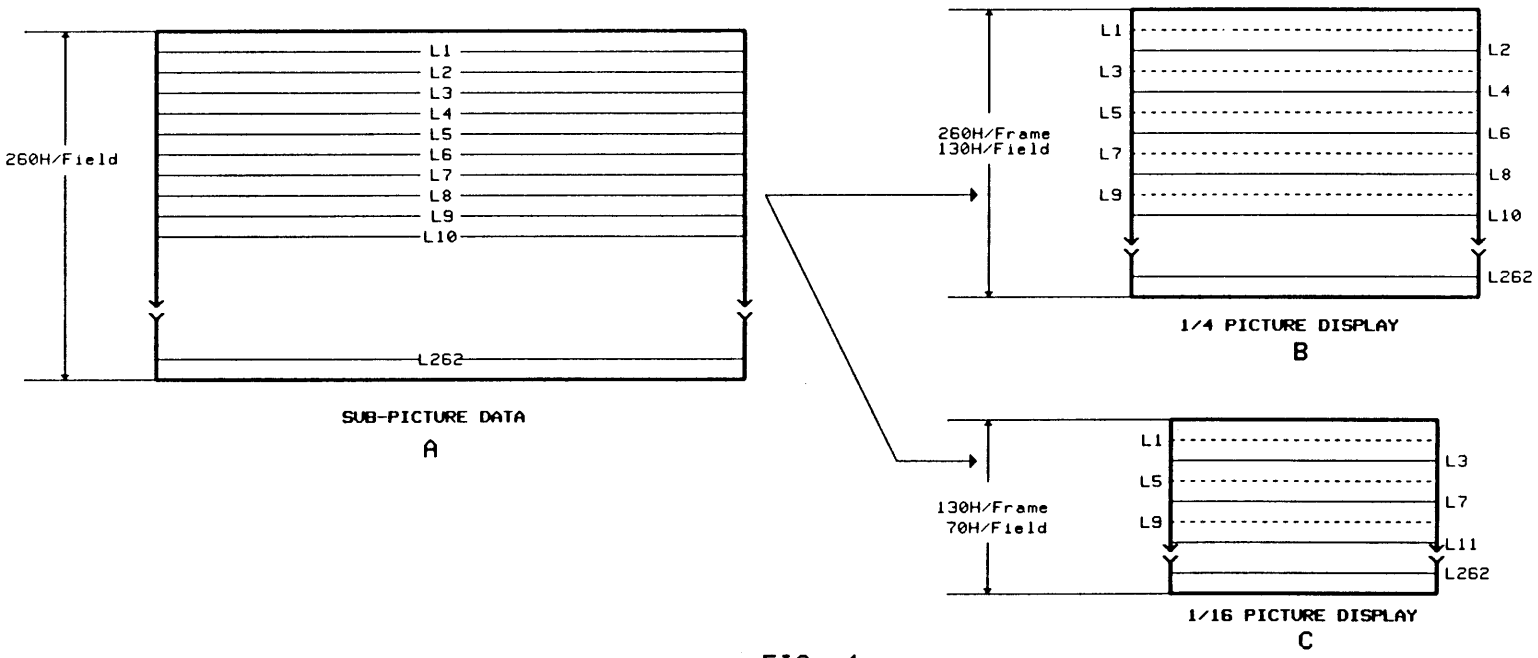


FIG. 4

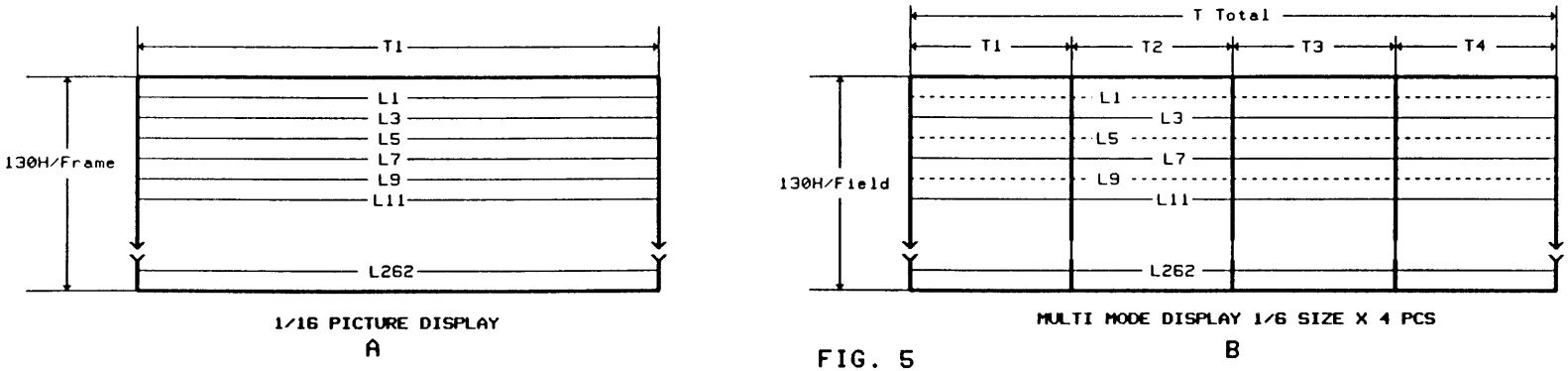


FIG. 5

TABLE ONE
GATE ARRAY PIN NAMES AND FUNCTIONS

PIN	NAME	I/O	FUNCTIONS
1	VDD	I	+5V Power Supply
2	RST	I	Hardware Reset
3	VDD	I	+5V Power Supply
4	VD	I	Vertical Sync Input for Display
5	HD	I	Horizontal Sync Input for Display
6	CS	I	Clamping Pulse Input
7	PVD	I	Vertical Sync Input for Writing
8	PHD	I	Horizontal Sync Inpt for Writing
9	DATA	I	CPU Interface Data Input
10	CK	I	CPU Interface Clock Input
11	LATCH	I	CPU Interface Latch Input
12	R	O	Output for Pedestal Clamping Time Constant
13	C	I	Input for Pedestal Clamping Time Constant
14	NTSCN	I	NTSCN/PAL Switching
15	VSS	I	GND
16	POSCI	I	Display OSC Circuit Input
17	POSCO	O	Display OSC Circuit Output
18	CONCKN	I	Clock Source Switching
19	COSCI	I	Writing OSC Circuit Input
20	COSCO	O	Writing OSC Circuit Output
21	VSS	I	GND
22	YSOUT	I	YS Signal Output
23	OTR5	O	R-Y Output (MSB)
24	OTR4	O	R-Y Output
25	OTR3	O	R-Y Output
26	OTR2	O	R-Y Output
27	OTR1	O	R-Y Output
28	OTR0	O	R-Y Output
29	OTB5	O	B-Y Output
30	OTB4	O	B-Y Output
31	OTB3	O	B-Y Output
32	OTB2	O	B-Y Output
33	OTB1	O	B-Y Output
34	OTB0	O	B-Y Output (LSB)
35	OTY5	O	Y Output (MSB)
36	OTY4	O	Y Output
37	OTY3	O	Y Output
38	OTY2	O	Y Output
39	OTY1	O	Y Output
40	VSS	I	GND
41	VDD	I	+5V Power Supply
42	OTYO	O	Y Output (LSB)
43	MD00	I/O	Field Memo Data Y10 (LSB)
44	MD01	I/O	Field Memo Data Y11
45	MD02	I/O	Field Memo Data Y12
46	MD03	I/O	Field Memo Data Y13
47	MD04	I/O	Field Memo Data Y14
48	MD05	I/O	Field Memo Data Y15 (MSB)
49	MD06	I/O	Field Memo Data Y20 (LSB)
50	MD07	I/O	Field Memo Data Y21

PIN	NAME	I/O	FUNCTION
51	MD10	I/O	Field Memory Data Y22
52	MD11	I/O	Field Memory Data Y23
53	MD12	I/O	Field Memory Data Y24
54	MD13	I/O	Field Memory Data Y25 (MSB)
55	MD14	I/O	Field Memory Data R-Y0 (LSB)
56	MD15	I/O	Field Memory Data R-Y1
57	MD16	I/O	Field Memory Data R-Y2
58	MD17	I/O	Field Memory Data R-Y3
59	MD20	I/O	Field Memory Data R-Y4
60	MD21	I/O	Field Memory Data R-Y5 (MSB)
61	MD22	I/O	Field Memory Data B-Y0 (LSB)
62	MD23	I/O	Field Memory Data B-Y1
63	MD24	I/O	Field Memory Data B-Y2
64	MD25	I/O	Field Memory Data B-Y3
65	VDD	I	+5V Power Supply
66	VSS	I	GND
67	MD26	I/O	Field Memory Data B-Y4
68	MD27	I/O	Field Memory Data B-Y5 (MSB)
69	A0	O	Field Memory Address (LSB)
70	A1	O	Field Memory Address
71	A2	O	Field Memory Address
72	A3	O	Field Memory Address
73	A4	O	Field Memory Address
74	A5	O	Field Memory Address
75	A6	O	Field Memory Address
76	A7	O	Field Memory Address
77	A8	O	Field Memory Address
78	A9	O	Field Memory Address
79	A10	O	Field Memory Address
80	A11	O	Field Memory Address
81	A12	O	Field Memory Address
82	A13	O	Field Memory Address
83	A14	O	Field Memory Address (MSB)
84	TEST	I	IC Check Terminal
85	R/W	I	Field Memory Write Control
86	SOFTCN	I	Picture Positionl Software Switch
87	ME2P	I	Capicity Switching
88	PD0	I	AD Converter Data Input (LSB)
89	PD1	I	AD Converter Data Input
90	VSS	I	GND
91	VDD	I	+5V Power Supply
92	PD2	I	AD Convertert Data Input
93	PD3	I	AD Convertert Data Input
94	PD4	I	AD Convertert Data Input
95	PD5	I	AD Convertert Data Input (MSB)
96	ADCK	O	AD Convertert Clock Output
97	MPY	O	Multiplexer Y Signal Selection
98	MPR	O	Multiplexer R-Y Signal Selection
99	MPB	O	Multiplexer R-Y Signal Selection
100	CLMP	O	Pedestal Clamping Pulse Out

NOTES

VI.

MTS BROADCASTING SYSTEM

MTS BROADCASTING SYSTEM

The North American audio multiplex broadcasting system allows simultaneous broadcasting of a monophonic sound, stereophonic sound (hereafter called stereo sound) and a separate audio program sound (hereafter called SAP).

In this system, MTS carves four information channels out of the 120KHz audio baseboard, hence the term multichannel, instead of merely stereo. Listed below is the layout of the four channels.

Main Channel (mono)

The main channel is the same as current broadcast systems. Here we have good old mono information, with a few kilohertz sliced off the the top end to allow room for the MTS pilot, at 15.734kHz (the horizontal scan rate). Deviation is $\pm$ 25kHz, with a pre-emphasis of 75us.

Noise reduction is not employed considering the compatibility of conventional receivers.

1st SUB Channel (stereo)

This channel is double sideband, suppressed carrier AM, just like FM MPX, provided for stereo broadcasting. L-R signal (which is a difference signal between the L and R signals) is audio bandwidth restricted to about 13kHz. The suppressed carrier's frequency is 31.47kHz, twice the horizontal scan rate which also happens to be the stereo pilot in the system. To reduce noise and buzz a dbz-NR system is included.

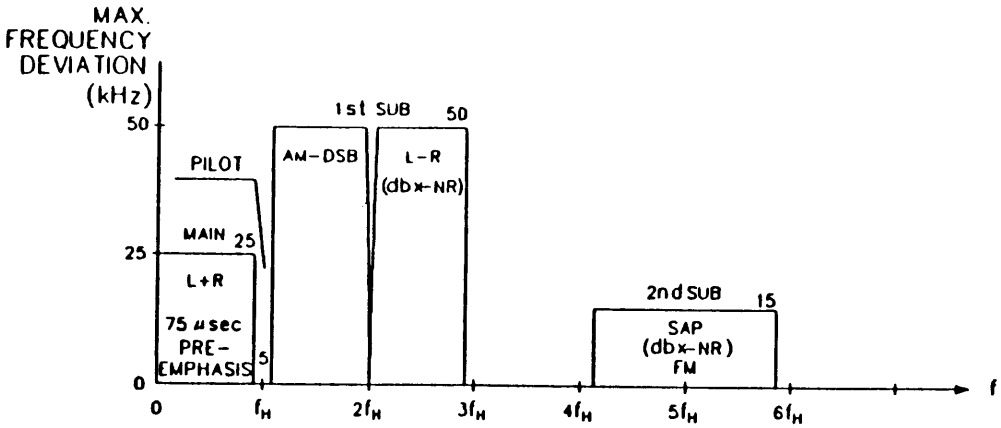
2nd SUB Channel (SAP)

To broadcast a second language, or whatever the station wishes a SUB channel is produced. It's FM, with an audio bandpass of 50Hz to 10kHz, centered on a carrier of 78.67kHz (5fH). It also employs the same type dbx-NR system since noise is relatively high.

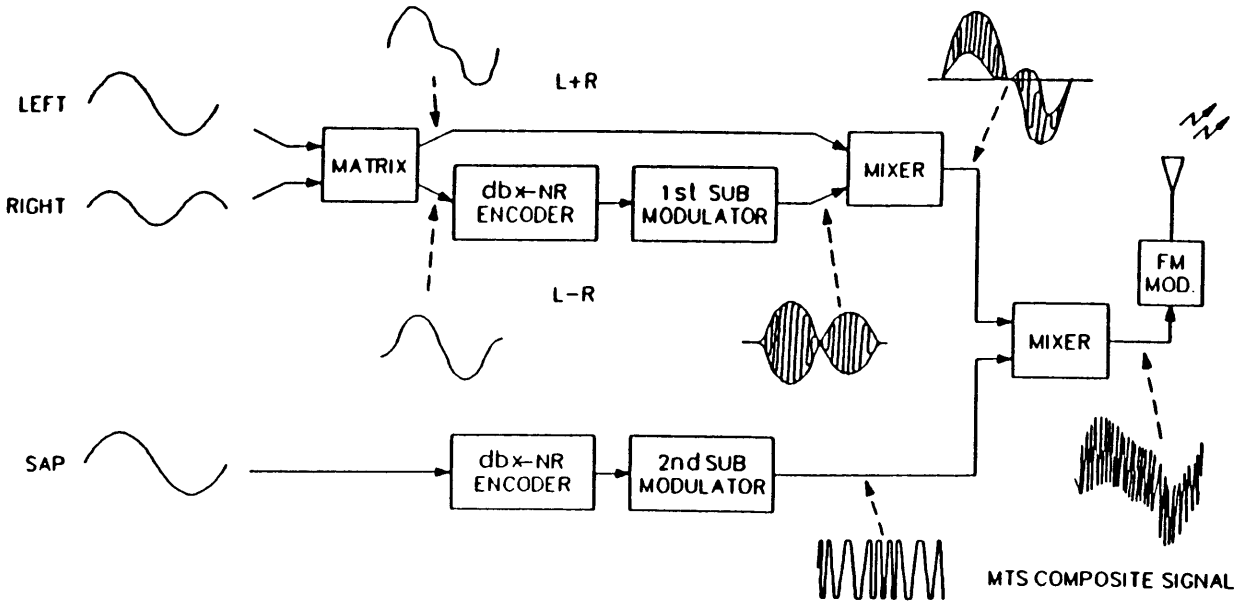
Stereo Pilot Signal

A pilot signal is added on the transmission side to inform that the signal being broadcasted has stereo information for the reception side. The frequency of the pilot is 15.734kHz (fH).

MTS SYSTEM



Frequency spectrum



MTS DEMODULATOR CIRCUIT

In reception of the MTS broadcasting, a composite signal consisting of the main channel, 1st SUB channel signal, 2nd SUB channel signal and stereo pilot signal is developed from the SIF detector. The demodulator circuit separates these signals, demodulates the separated signals, selects audio signals depending upon the signal content (stereo or SAP) and incoming switching commands, and displays the signal contents through LED's. In this chassis, ICG01 is employed to handle the above functions in addition to the volume and tone control functions.

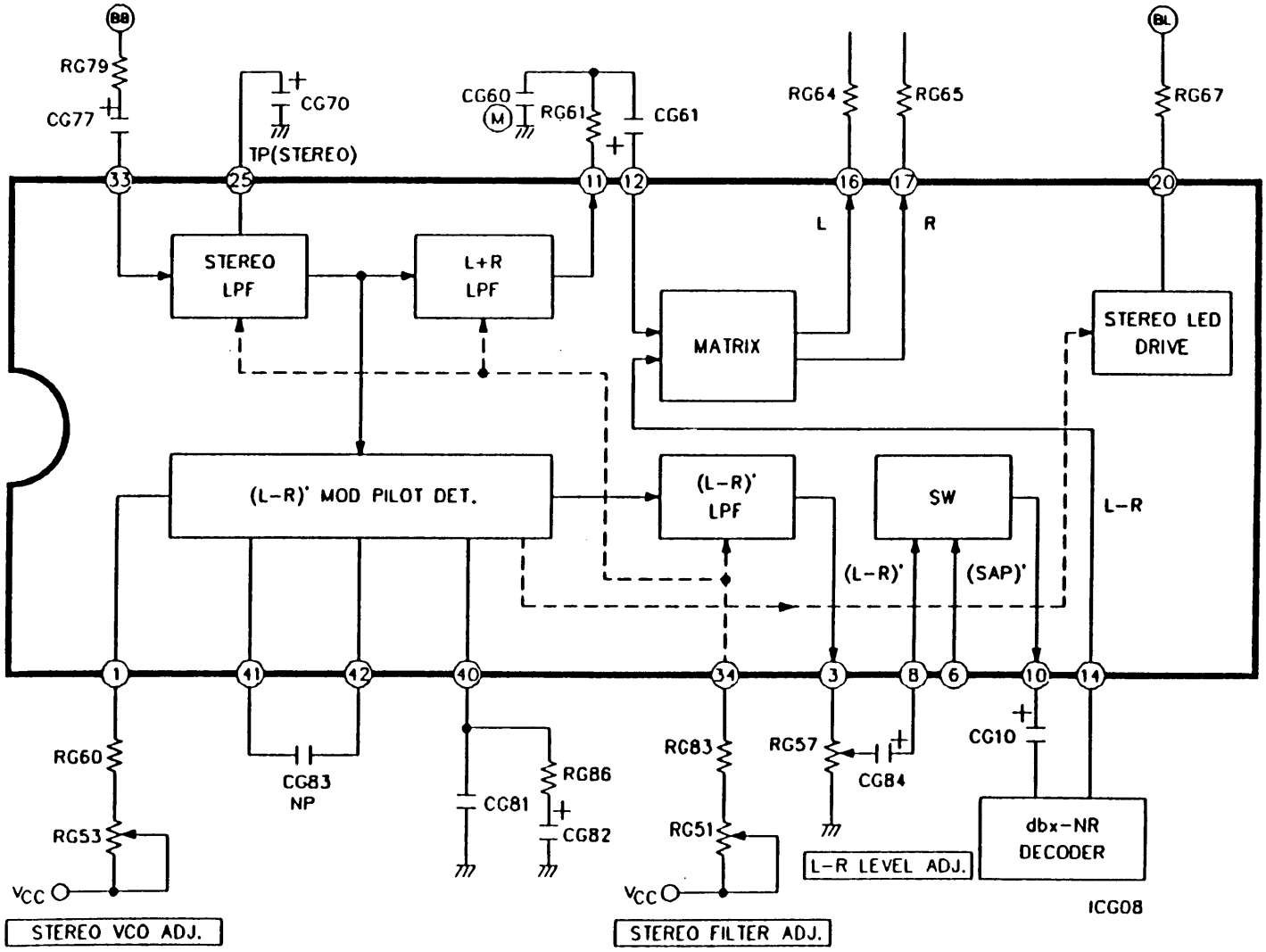
Theory of Operation

During the reception of a mono signal or in the forced-mono mode, the composite signal applied to BB terminal of the MTS board inputs pin 33 of ICG01. Within the IC the signal is coupled through a stereo LPF that removes the SAP signal if present. The signal then passes through a (L+R) LPF and outputs at pin 11 for de-emphasis. It is then coupled back to the IC at pin 12 and enters a matrix circuit. The left and right channel output of the matrix in mono will be the same as the signal outputs from pins 16 and 17.

When receiving a stereo broadcast, the circuits up to the stereo LPF are the same as those of the main channel. The LPF output is demodulated into an AM signal and encoded by the dbx-NR and outputs at pin 3. The detected L-R signal is adjusted to a proper level by RG57 and inputs at pin 8. At pin 8 the signal is coupled to the switch circuit that selects stereo or the SAP signal. The output of the switch at pin 10 passes through the dbx-decoder ICG08 and then inputs at pin 14 as a true L-R signal for processing with the L+R signal in the matrix circuit. The R channel signal outputs at pin 17 and L channel outputs at pin 16.

In addition to the above circuits, a stereo identification circuit is provided to detect the stereo pilot signal. When a stereo signal is present, the identification circuit develops a high level voltage within the IC to the LED driver that outputs at piun 20 to activate the stereo LED.

STEREO DEMODULATOR BLOCK DIAGRAM



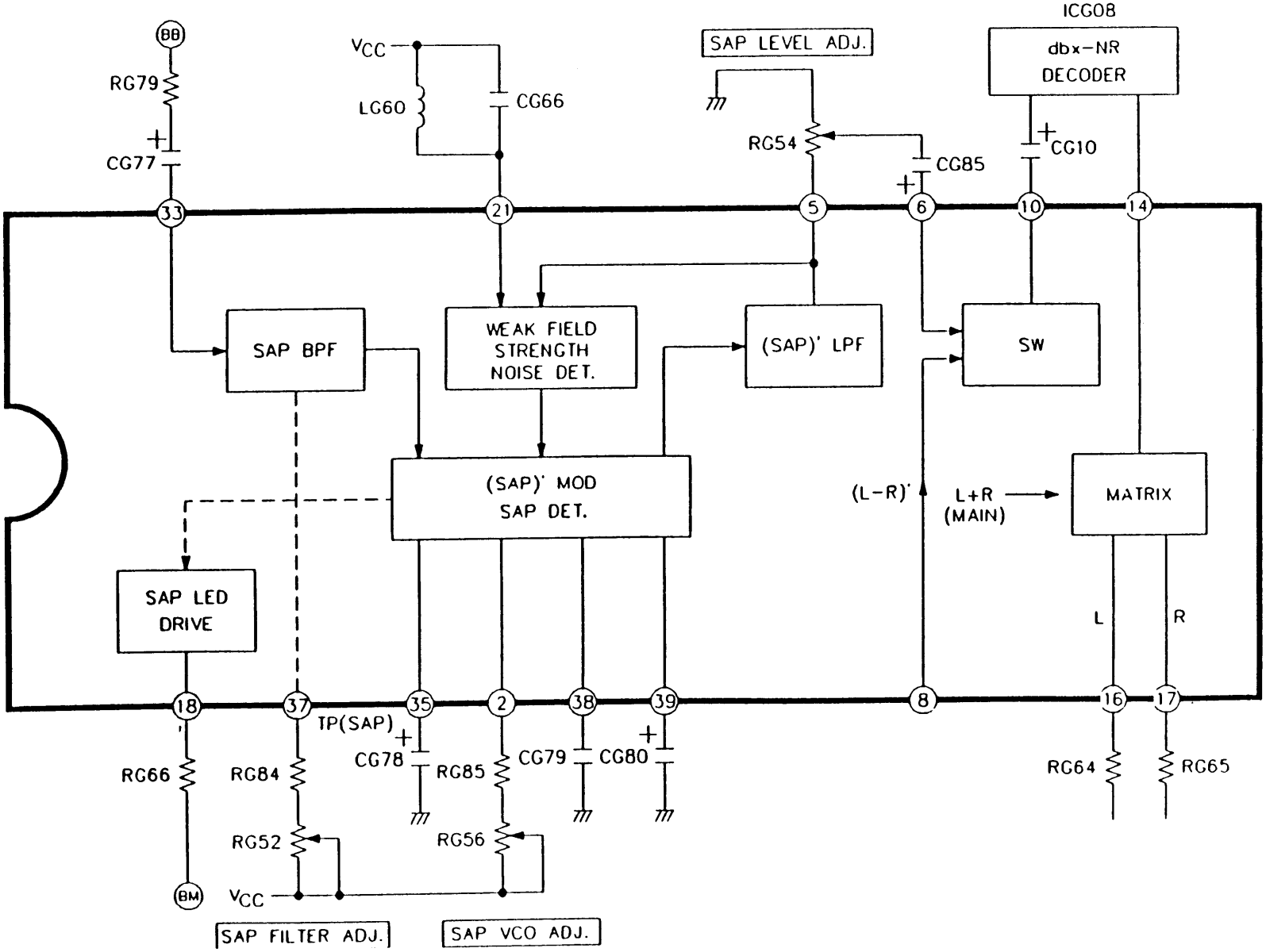
SAP DEMODULATOR CIRCUIT

The SAP signal is a frequency modulated signal with a carrier frequency of 5fH. It inputs at pin 33 of ICG01 and by passing through a 5fH BPF, only the SAP signal is extracted. Then the signal is frequency-detected and the output is coupled to pin 5 through a LPF. Resistor RG54 establishes the SAP level and the signal is coupled to the switch from pin 6. After the signal is selected with the switch, it inputs the same circuit as the one used for stereo signal (L-R) processing.

The SAP mode identification is carried out by detecting the 5fH carrier signal. The voltage developed by the carrier detector inputs the LED drive circuit and is resistive coupled from pin 18 to activate the LED.

To prevent erroneous operation of the SAP circuit when reception is weak, output noises developed after the SAP LPF enters the WEAK FIELD STRENGTH NOISE DETECTOR. If the signal-to-noise ratio is low due to weak reception, pin 19 is set high (4-5 V) keeping the unit in the SAP mode.

STEREO DEMODULATOR BLOCK DIAGRAM

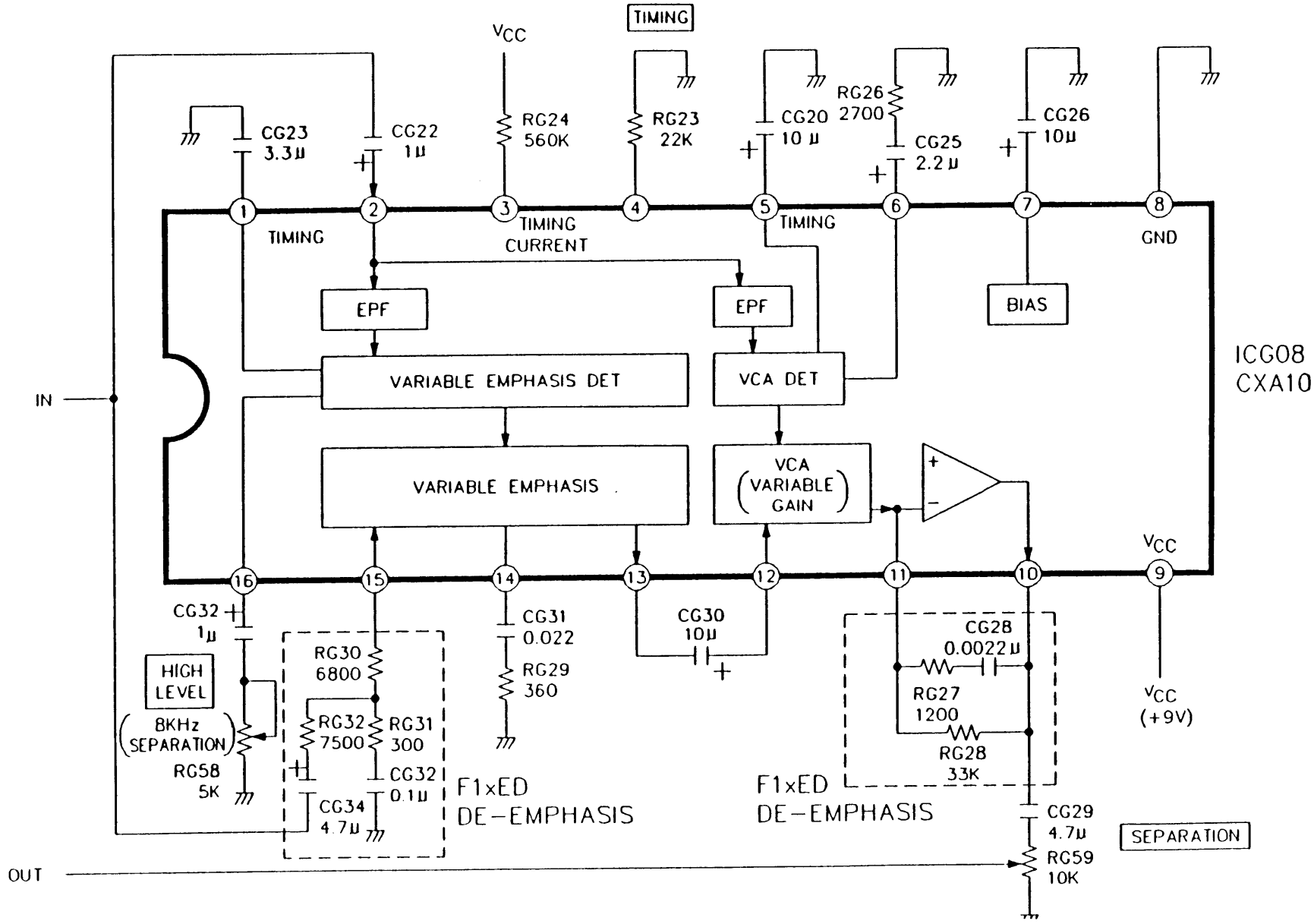


dbx-NR DECODER

The input signal from pin 10 of ICG01 splits before the decoder, and one path inputs a fixed de-emphasis circuit consisting of RG30, RG31, RG32 and CG32, CG34. At pin 15 this signal enters a variable de-emphasis circuit. Pin 13, the de-emphasis output is coupled across CG30 and inputs the Voltage Control Amplifier (VCA) at pin 12. Next, the output is subject to current-voltage conversion in the OP-amp, and then at pin 10 outputs as a decoded signal through another fixed de-emphasis circuit made up of RG27, RG28, and CG28.

The transmission function and gain of the variable de-emphasis circuit and VCA are controlled by the second signal path to pin 2 in an effective value detector circuit. Each value detector circuit gives a weighing to the input signal by coupling the signal through a BPF. The effective value of the signal is detected, thereby obtaining the control signal.

dbx-NR DECODER



MODE SWITCH CIRCUIT LOGIC

Mode switching for Stereo, SAP, and Mono is conducted by applying control voltages developed in ICA01 to pins 13 and 15 of ICG01. The table below shows the voltages at ICG01 pins 16 (L), 17 (R), 5 (SAP-out), and LED display for various mode settings.

MODE	MODE SELECTOR	LOGIC SELECTOR		OUTPUT			LED DISPLAY	
		(BP)	(BO)	(16) (L)	(17) (R)	(5) (SAP OUT)	STEREO	SAP
STEREO	STEREO	4.6V	0V	L	R	–	O	X
	SAP	0.4V	0V	L	R	–	O	X
	MONO	4.6V	3.7V	L + R	L + R	–	X	X
MONO	STEREO	4.6V	0V	L + R	L + R	–	X	X
	SAP	0.4V	0V	L + R	L + R	–	X	X
	MONO	4.6V	3.7V	L + R	L + R	–	X	X
STEREO SAP	STEREO	4.6V	0V	L	R	SAP	O	O
	SAP	0.4V	0V	SAP	SAP	SAP	O	O
	MONO	4.6V	3.7V	L + R	L + R	SAP	X	X
MONO SAP	STEREO	4.6V	0V	L + R	L + R	SAP	X	O
	SAP	0.4V	0V	SAP	SAP	SAP	X	O
	MONO	4.6V	3.7V	L + R	L + R	SAP	X	X

VII.

AUDIO PROCESSING

AUDIO CIRCUIT OUTLINE

SIF CIRCUIT

The SIF circuit obtains the audio information by first detecting the IF signal supplied from the SAW filter Z101 and extracting the 4.5Mhz. component. The signal is then FM detected and the audio output is coupled to the Audio Multiplex IC.

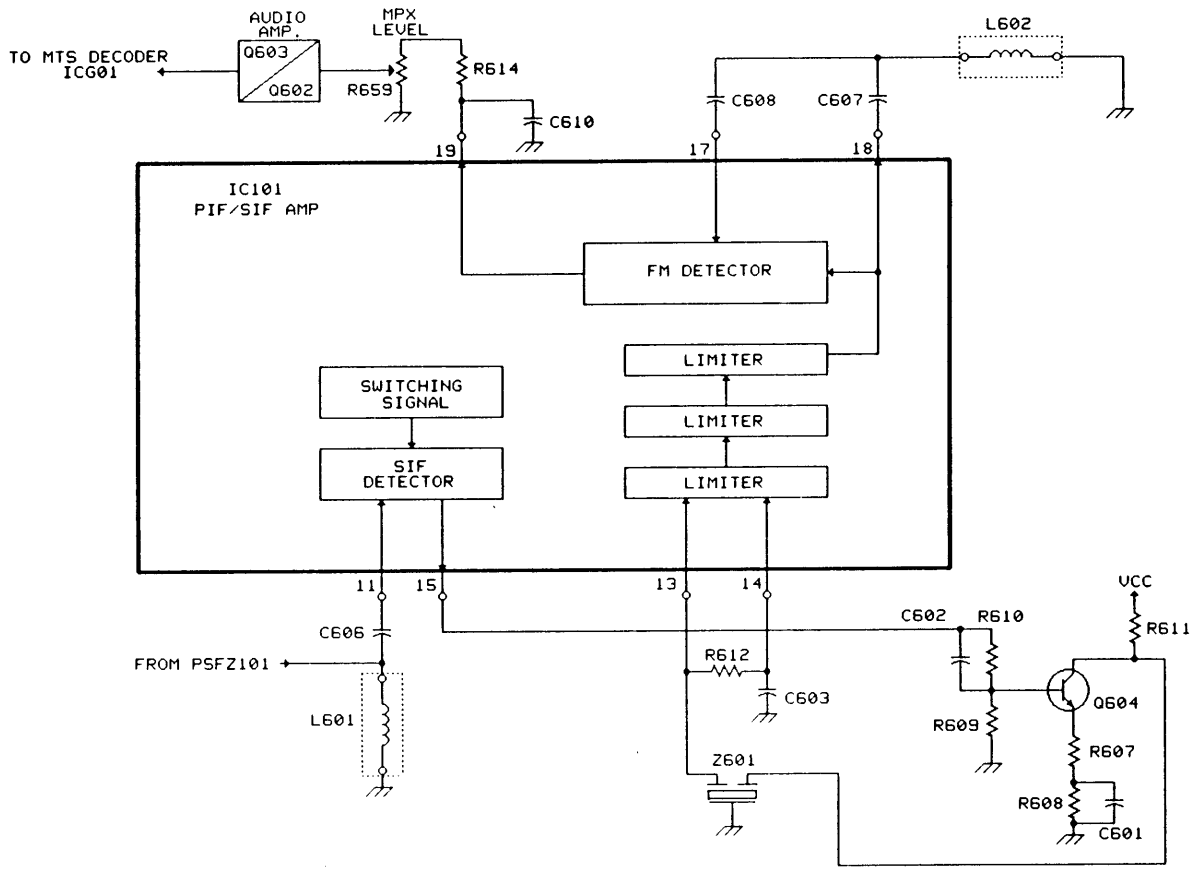
PLL sync detection within IC101 is used to maintain proper phase relationship to the video which prevents buzzing from occurring due to video overmodulation.

Theory of Operation

The IF signal which is band-limited by the SAW filter Z101 inputs IC101 at pin 11 and the 4.5Mhz component is extracted by the detector circuit in the IC. The 4.5Mhz signal outputs at pin 15 and is coupled to the amplifier Q604. The output at the collector is then coupled to the 4.5Mhz BPF, Z601 to increase sensitivity and to eliminate noise. This signal returns to IC101 at pin 13 to a limiter network within the IC that prevents amplitude changes regardless of input strength.

The signal is coupled through a FM detection circuit that consists of the externally tuned circuit of C607, C608, and L602. The developed audio signal outputs IC101 at pin 19 to be amplified by Q602 and emitter follower Q603. The audio signal outputs the PIF/SIF board at connector AH and is derectly coupled to the audio multiplex input of ICG01 in the MTS PCB as input line BB.

SIF CIRCUIT


AUDIO AMP.
Q603
Q602
MPX LEVEL
TO MTS DECODER ICG01
R659
R614
C610
L602
C608
C607
19
17
18
IC101
PIF/SIF AMP
FM DETECTOR
LIMITER
LIMITER
LIMITER
SWITCHING SIGNAL
SIF DETECTOR
11
15
13
14
VCC
C602
R610
R611
C606
FROM PSFZ101
R612
C603
Q604
L601
R609
Z601
R607
R608
C601

AUDIO OUTPUT

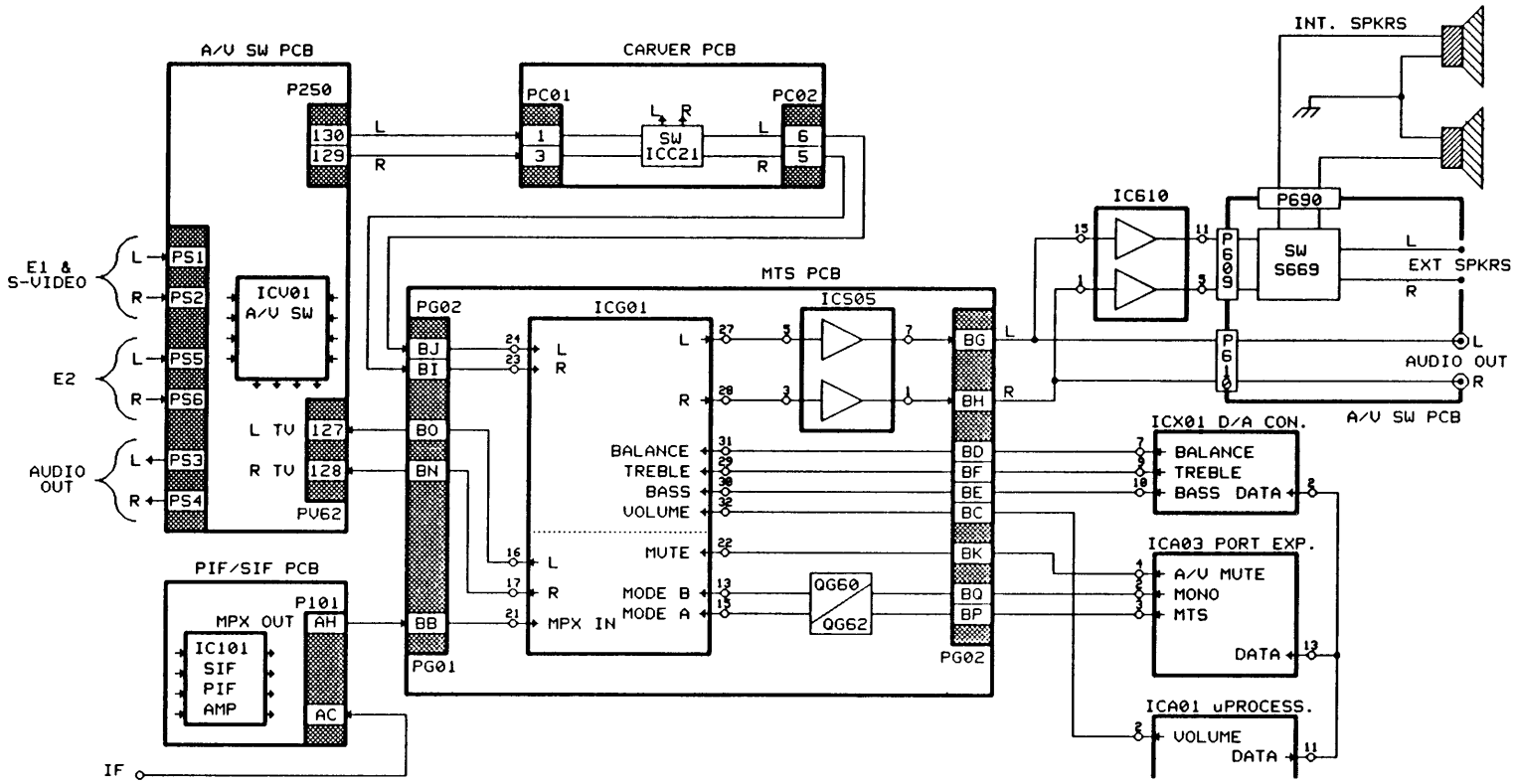
An audio composite signal outputs from the PIF-SIF unit and inputs at terminal BB of the audio multiplex unit where the signal is processed with-in the audio multiplex demodulator , ICG01. The demodulated audio signal outputs from terminals BO and BN to the A/V switch unit which selects an external audio source or the TV audio signal. Through terminals BJ and BI the audio signal again inputs the Audio Multiplex Unit. Inside the unit, volume control is carried out by a PWM signal developed from the microcomputer (ICA01). Balance control, bass, and treble control is set by the DC control voltage from the D/A converter (ICX01).

Next, the audio signals input terminals BG(L) and BH(R) after passing through amplifier ICS05. From the Audio Multiplex Unit both signals are split. One set of signals is applied to the variable output terminals at the back of the TV set. The other set of signals inputs pins 1 and 15 of IC610, which is the Audio Output IC.

The outputs of the Audio Output IC are pin 11 Lch and pin 5 Rch, they input the speaker switch (on the A/V SW PCB) to drive either the internal speakers or external speakers depending on the setting of S669 located in back of TV set.

NOTE: The Fixed Audio Out does not go through the Audio Circuit, it is taken right out of the A/V Switching IC.

AUDIO CIRCUIT BLOCK DIAGRAM



VOLUME, TONE CONTROL CIRCUIT

This circuit adjusts the volume, bass, treble, and sound balance. The control circuits are packaged in ICG01 (TA8622N). The volume control is carried out with a Pulse Width Modulation (PWM) signal coupled from the microprocessor ICA01. Bass, treble, and balance controls are carried out by DC voltages developed in ICX01 (D/A Converter IC).

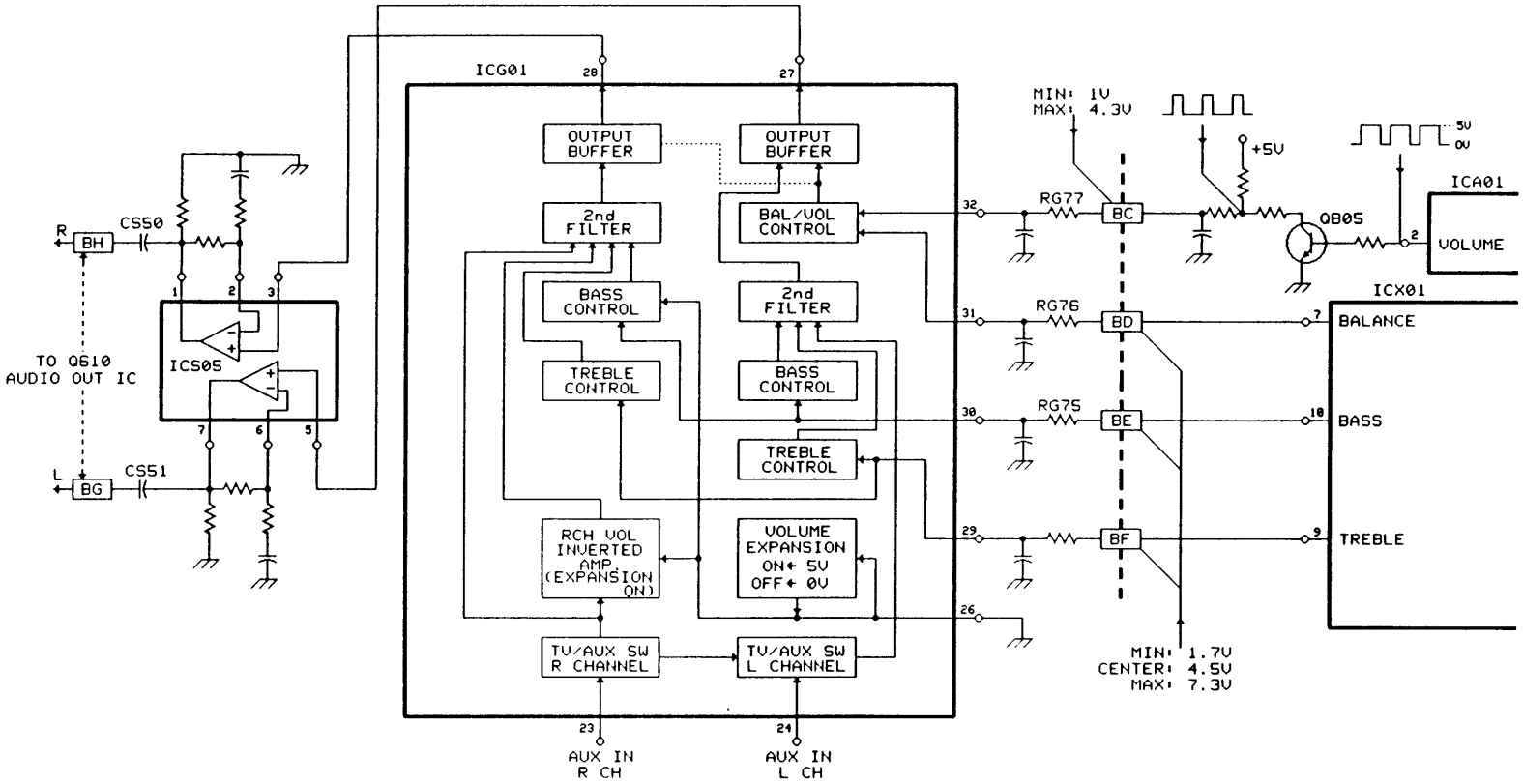
THEORY OF OPERATION

ICA01 on the Main board, develops the PWM signal and outputs it at pin 2. The signal is inverted by QB05, integrated, and converted into a DC voltage. The DC voltage is applied to pin 32 of ICG01 to control the sound volume. Raising or lowering of the volume level is carried out by varying the pulse width.

The bass, treble, and balance controls are directed by the D/A converter ICX01 which converts the digital signals developed in the microcomputer ICA01 into DC voltages. These DC control voltages input ICG01 at pins 29, 30, and 31.

The audio signal with the volume level and tone quality adjusted, outputs ICG01 at pins 27 (L) and 28 (R), and inputs the amplifier ICS05. This IC has a signal gain of about 2.6 times. Left and Right channels then input the variable output circuit and the main amplifier (Q610) by connectors BG and BH.

AUDIO CONTROL CIRCUIT



NOTES

VIII.

CARVER AUDIO

CARVER SONIC HOLOGRAPHY

CARVER SONIC HOLOGRAPHY is a stereo audio system that is designed to produce a sound field that simulates listening to actual events. This is accomplished by removing the defect of sound fields becoming narrow due to speaker crosstalk or positioning becoming vague if the distance between left and right speakers is especially close. (NOTE: Carver Audio is not designed to work with external speakers).

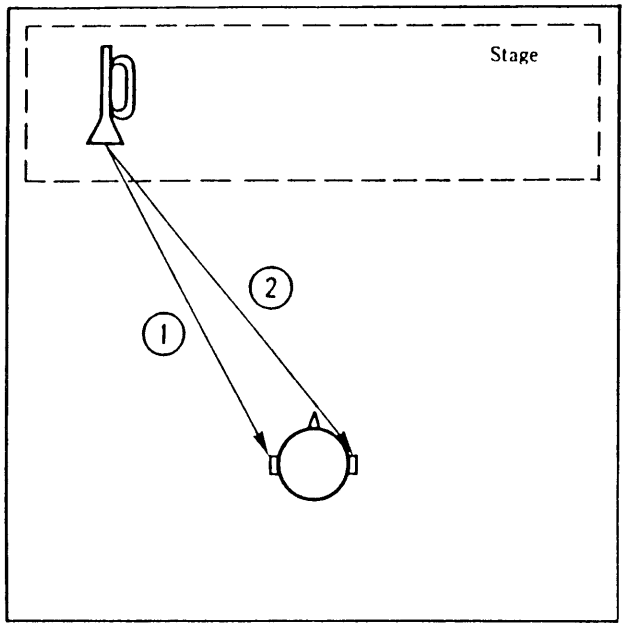
Principle of Operation

Fig. 1 illustrates the condition as sound is transmitted to a listener in a live concert. Location of the sound source is known due to the time or volume difference between sounds (1) and (2) transmitted to the left and right ears. Note that a listener continuously hears two sounds from each sound source.

Fig. 2 shows stereo playback with 2 speakers. The source of sound was recorded using two microphones positioned at each ear of the listener, (Fig. 1). Therefore, Sound (1) outputs from the left speaker and Sound (2) from the right speaker. In this case however, four sounds are actually heard by the listener as illustrated. These (1)' and (2)' sounds are crosstalk components, which are excessive sounds and may distort the location of the sound image. This causes the listener to imagine that the sound image is in a narrowed location as illustrated.

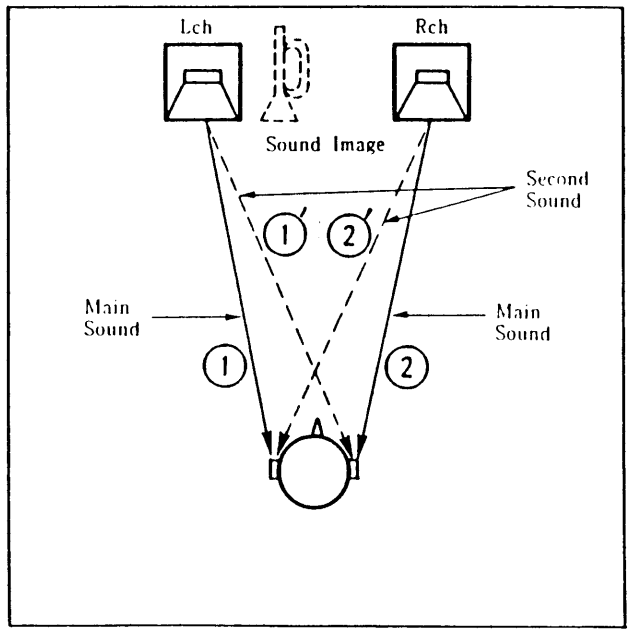
Fig. 3 shows the state of stereo playback using the Carver Sonic Holography. Cancellation Signals (C1) and (C2) are produced to elliminate cross talk components (1)' and (2)'. The cancellation signals are produced when a portion of each channel is time delayed and outputs from the opposite side speaker so that they negate the crosstalk components at the listening position. As a result, the listener experiances a sound image that has expanded to the location shown in Fig. 3 and the same sound field as in Fig. 1 is simulated.

CARVER SONIC HOLOGRAPHY



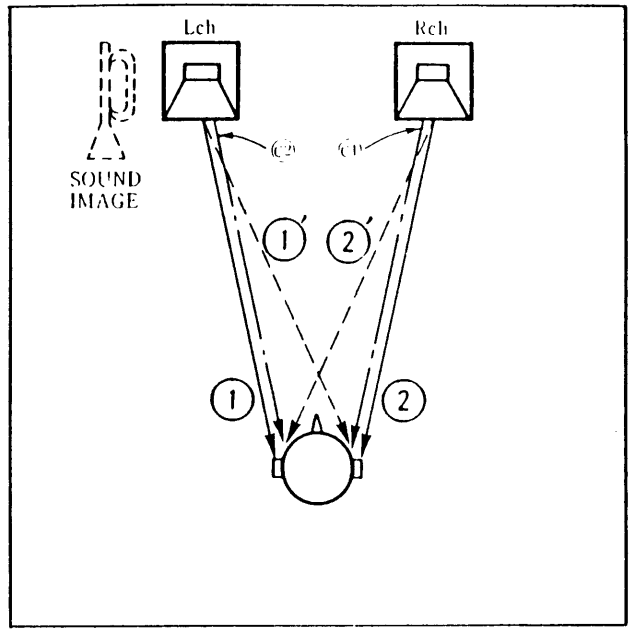
LIVE EVENT

FIG. 1



STEREO PLAYBACK

FIG. 2



CARVER AUDIO

FIG.3

CARVER SONIC HOLOGRAPHY (cont)

The block diagram of the Sonic Holography Circuit is shown in Fig. 4. To achieve the cancellation signals needed both L&R Channels will go through "mirror" circuitry in the Carver PCB. Portions of the audio signal are routed through a H.P.F., a delay circuit, a second H.P.F., a second delay circuit, a L.P.F., a third delay circuit, and an inversion amplifier. This provides the cancellation signals information that will be shared by the left and right channels.

These combined signals (L ch. Audio + R ch. Cancellation Signal and R ch. Audio + L ch. Cancellation Signal) now input the equalizer circuits. These circuits will correct any changes in audio signal frequency characteristics that have occurred due to the addition of the Cancellation Signal. The combined signals now output the Carver PCB and are fed back through the Main PCB to input the MTS Decoder PCB.

The Delay Time, the gain of the inversion amplifier and characteristics of the equalizer circuit are determined by the distance between the speakers of the set and the distance to the listening point.

CARVER AUDIO BLOCK DIAGRAM

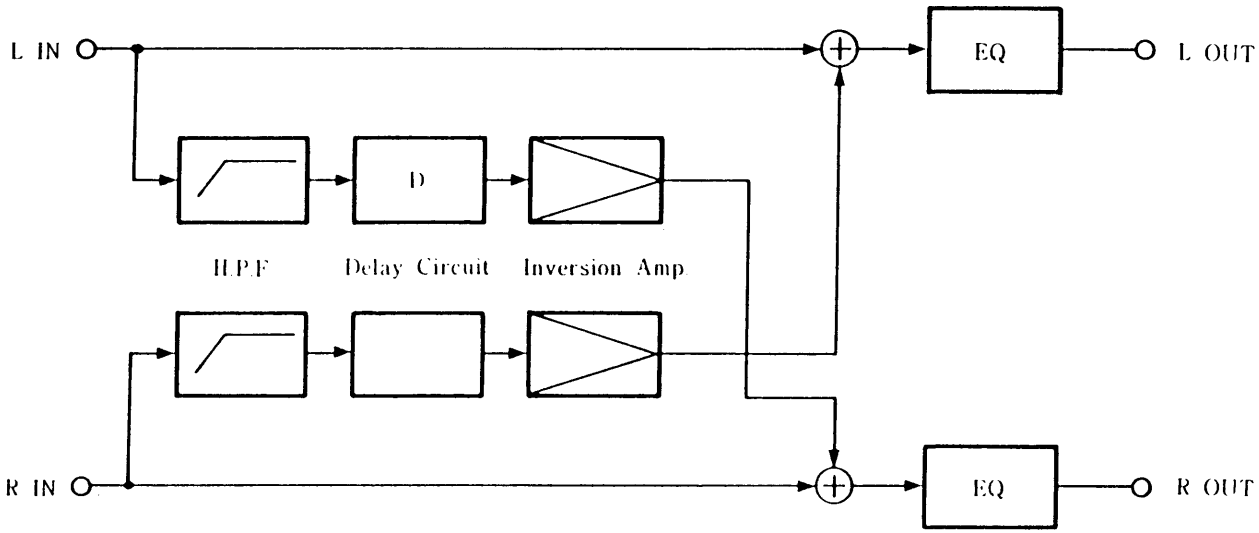


FIG. 4

OPERATION OF CARVER AUDIO CIRCUITS

Because the Carver Board uses "mirror" circuitry to achieve the cancellation signals needed for both L&R Channels, only the left channel will be discussed.

The Left Channel signal entering the Hologram Section will go through Buffer Amp. 1 and the output will split into two paths. Path number **(1)** goes through a frequency attenuation circuit, this output is resistive coupled to an Adder Circuit. The second path goes through H.P.F.1 (300 Hz cutoff) which will cutoff the base tones.

The output of H.P.F.1 splits into two paths. Path number **(2)** is resistance coupled to the Inversion Amp. The second path goes through Delay Circuit 1 (D1), with a delay of 44 us the full audio range is delayed.

The output of D1 splits into two paths. Path number **(3)** is resistance coupled to the Invertion Amplifier. The second path goes through H.P.F.2 (2 KHz cutoff), D2 (510 us), and L.P.F.1 (2 KHz cutoff). Together H.P.F.2 and L.P.F.1 make up a B.P.F. with a center frequency of 4 KHz.

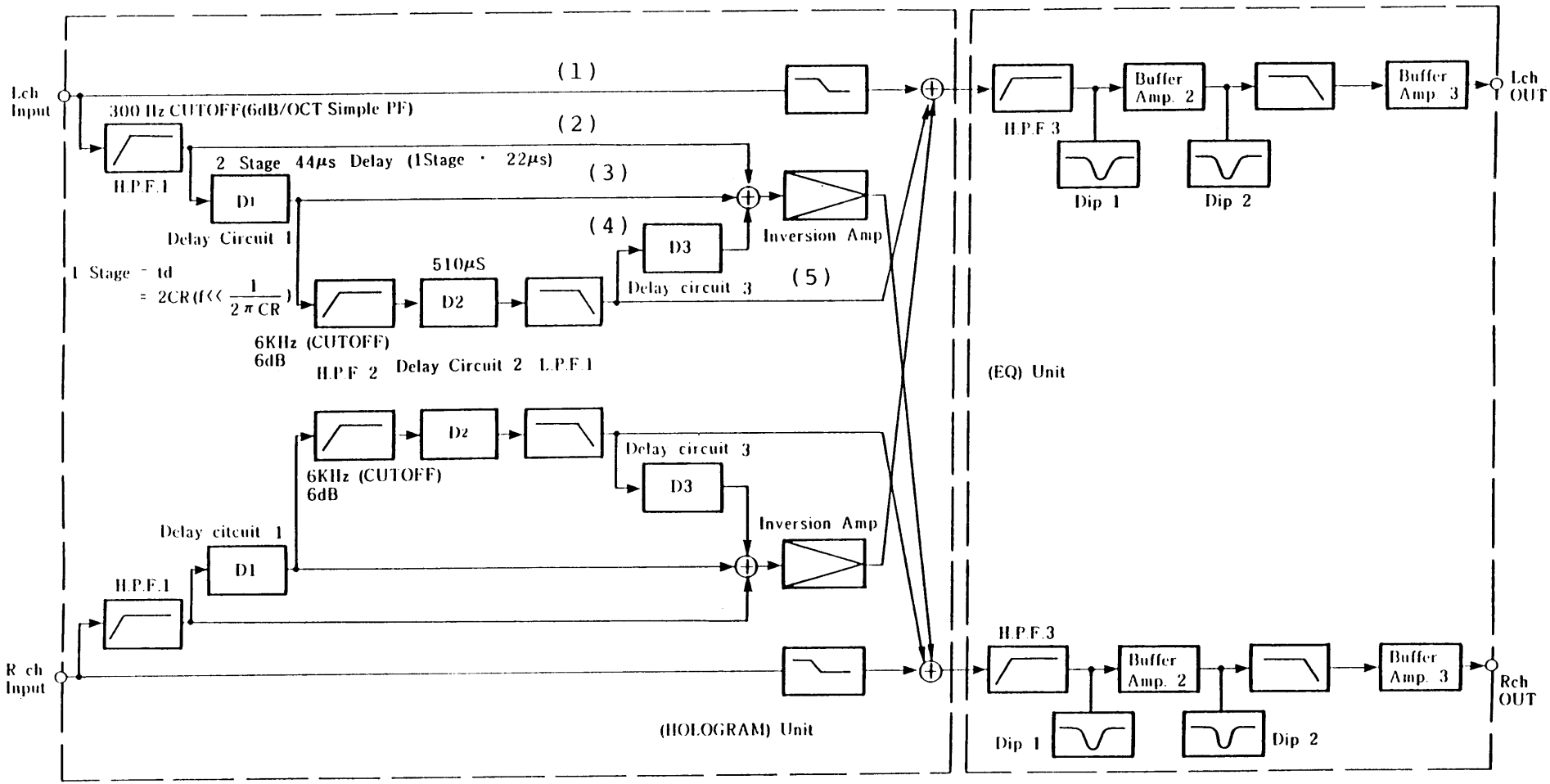
The output of L.P.F.1 splits into two paths. Path number **(4)** goes through D3 (75 us) and the output is resistance coupled to the Invertion Amplifier, this combined output is the L Ch cancellation sigal and will be added to the Right Channel path at the Right Ch. Adder Circuit.

Path number **(5)** is resistance coupled to the Adder Circuit, the output of wich is the L Ch out and along with the R Ch Cancellation Signal will enter the EQ Section.

The left channel enters the EQ Section and goes through H.P.F.3 (40 Hz cutoff) and L.P.F.2 (12 KHz cutoff), together they make up a B.P.F. with a center frequency of about 6 KHz. At the same time, the signal is also passing through Dip 1 (2 KHz dip) and Dip 2 (7.5 KHz dip), together they make up a wide range B.E.F.

The processed signal will now go through Buffer Amp.3 and the output is capacitive coupled to the Switching IC before exiting the Carver PCB.

CARVER AUDIO BLOCK DIAGRAM



NOTES

IX.

VERTICAL DEFLECTION

VERTICAL DEFLECTION CIRCUIT

The Vertical Deflection Circuit of the projection television is basically identical to that of the X-63 Chassis except for the following points:

(1). Three deflection coils are provided since three CRT's are used.
(2). Should the unit loose vertical deflection, a protective circuit is provided to keep the fluorescent screen of the projection CRT from being burned.
(3). Vertical Linearity is adjustable.

The basic deflection circuit performs two main functions. That is to generate the Vertical Deflection Sawtooth and to provide the necessary power amplification to drive the Vertical Deflection Yoke. The Vertical Deflection Amplifier also provides the output for Vertical Retrace Blanking.

The Vertical Deflection Circuit used is a differential type amplifier. This circuit consist of two IC's, Q501 which contains a Vertical Sync Circuit, a Sawtooth Wave Generator, and a Differential Amplifier, and Q301 which contains a Pump-up Circuit and the Vertical Drive Output, see Figure 1. This Vertical Deflection Circuit supplies a sawtooth waveform current with good linearity to the Deflection Yoke, in synchronization with the Vertical Sync Signal.

VERTICAL DEFLECTION CIRCUIT

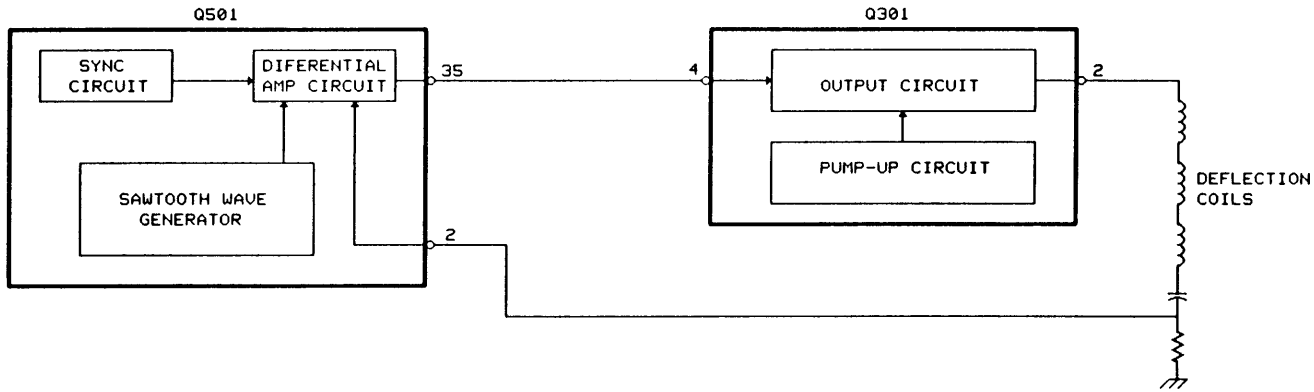


FIG. 1

VERTICAL DEFLECTION CIRCUIT (CONT.)

VERTICAL OUTPUT

The signal output from the Sawtooth Waveform Generating IC Q501 pin 35, enters the Vertical Output IC Q301 pin 4 (See figure 2). Here the input signal is amplified by the Vertical Driver Q2, then the signal is current amplified by a Single End Push-pull Output Amplifier consisting of Q3 & Q4. Q3 operates as the amplifier for the first half of the scanning period and allows a positive current to flow into the deflection yokes then Q4 operates for the later half of the scanning period and allows a negative current to flow into the yokes.

The impedance (DC resistance) of the deflection coils is maximum during the Scanning Period. On the other hand, the inductance becomes maximum during the Fly-back Period when it is necessary to reverse the polarity of the deflection current in a short time. Therefore, a high voltage supply is needed at this time. Since a constant high voltage supply will result in an increase of power consumption, a circuit that can switch the supply voltage from the Scanning Period to that of the Fly-back Period is desired.

The circuit that switches the voltage for the Scanning Period and the Retrace Period is called a **Pump-up Circuit**. The purpose of the Pump-up Circuit is to return the yoke current during retrace back to the output amplifiers by applying a high voltage only for the retrace period. The Pump-up Circuit is activated by triggering pin 5 of Q301 through R310 & C312 with a retrace pulse developed at pin 2.

VERTICAL DEFLECTION CIRCUIT

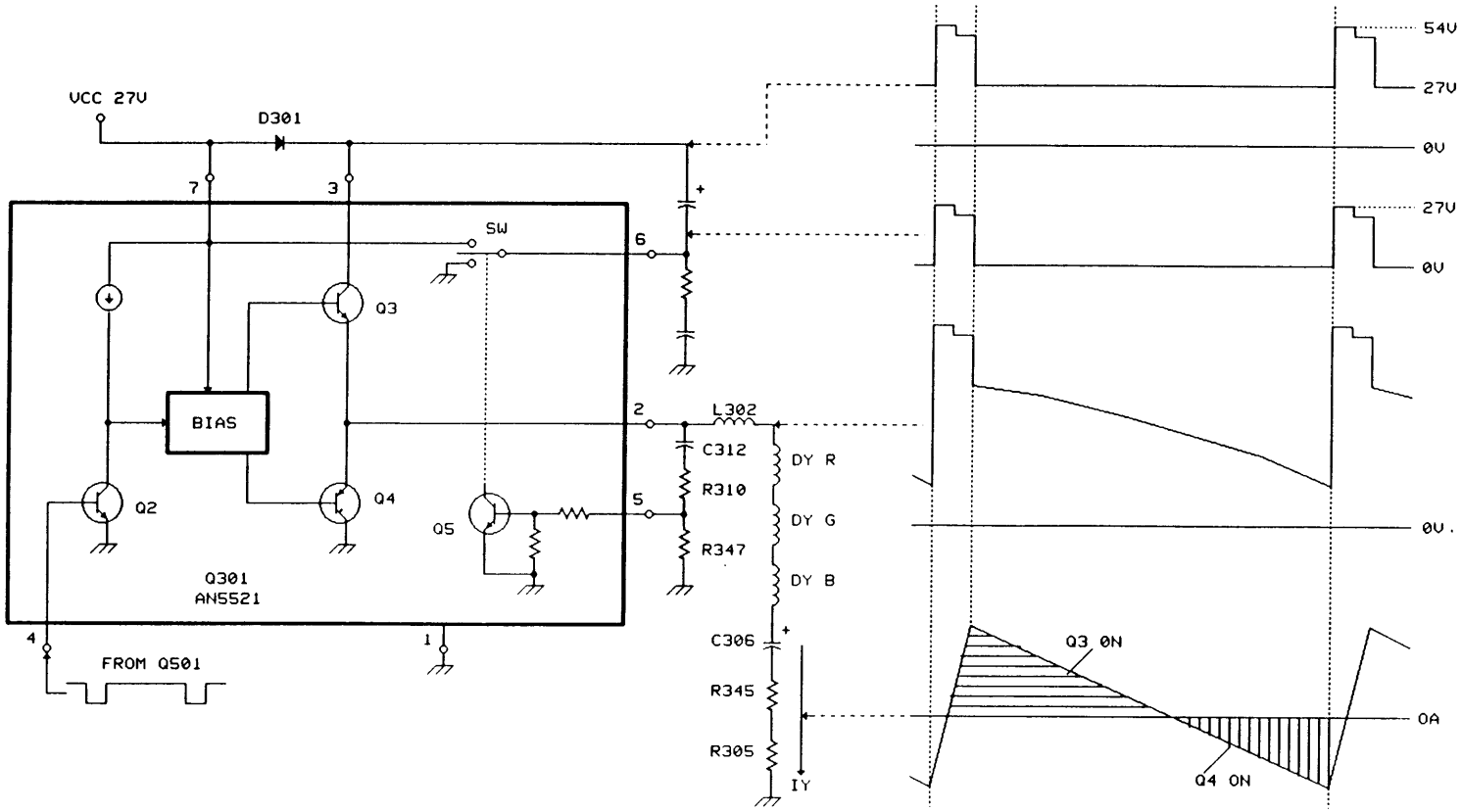


FIG. 2

VERTICAL DEFLECTION CIRCUIT (CONT.)

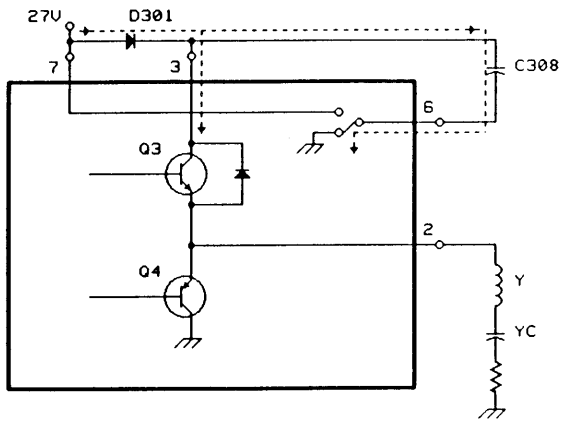
VERTICAL OUTPUT

In the Pump-up Circuit, during the Scanning Period (See Figure 3), the transistor switch inside Q301 connects pin 6 to ground. The 27V power input to pin 3 becomes equal to VCC-VF, (VF is the voltage drop across D301). This voltage is applied to the output stage Q3. During this time C308 is also charged up to that same potential.

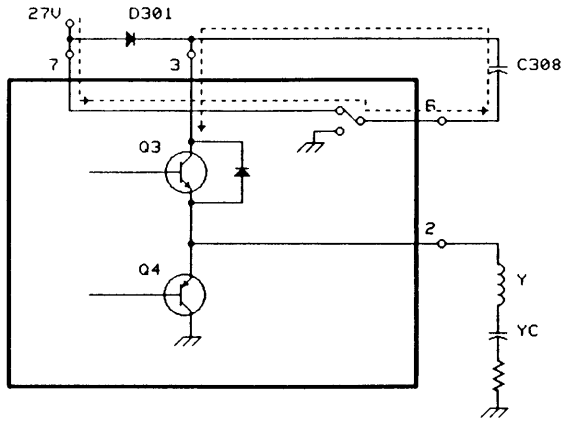
During the Retrace Period, the transistor switch connects Q301 pin 6 to pin 7(Power supply VCC). As a result, the output stage voltage at pin 3 becomes the sum of the voltage at pin 6 (VCC) and the voltage at C308 (VCC-VF), which will total up to (2VCC-VF). This condition will reverse bias D301 and turn it off.

The final outcome is that a power supply voltage of 27V is applied to the output stage for the Scanning Period and 54V for the Retrace Period. See Figure 4.

VERTICAL PUMP-UP CIRCUIT

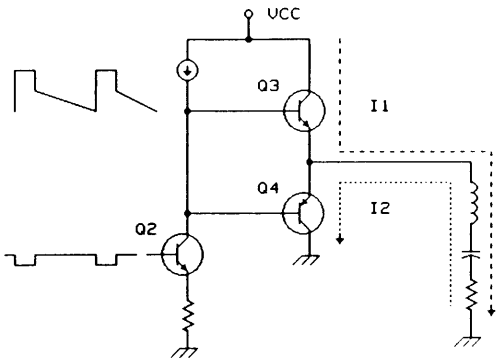


SCANNING PERIOD



FLYBACK PERIOD

FIG. 3



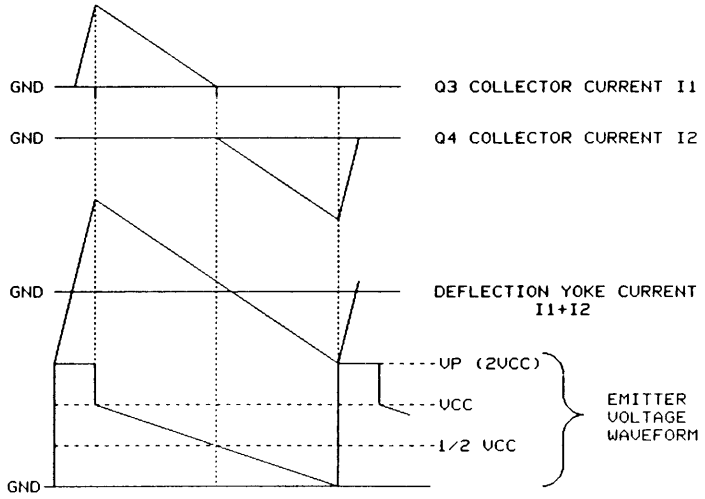


FIG. 4

LINEARITY CORRECTION OPERATION

S-CURVE CORRECTION

Because of the varying resistance produced by the yoke, a linear sawtooth of current in the yoke will result in stretching at the top and bottom of the raster. This can be compensated by intentionaly distorting the sawtooth into an S Shape. Since sawtooth current (deflection current) flows to the output capacitor C306, a parabolic voltage is available on either side. An S-curve voltage is produced by integrating this parabolic voltage at R306/C305 (See Figure 5). The sum of the Integration Circuit is fed back to Q501 pin 2 and thereby performing S-curve Correction.

UP-DOWN LINEARITY CORRECTION

Because the Vertical Deflection Circuit uses a differential amplifier system (See Figure 5), proper results are obtained during up-down linear correction by using the differential amplifier action between pins 1 and 2 of Q501. The correction voltage is then applied to the input of Q301 pin 4. R306 and C305 perform the integration of the S-shape voltage mentioned above and the sawtooth voltage generated at both ends of R345, the resulting parabolic voltage is also fed back to Q501 pin 2 to produce an "Upper expansion and lower compression" affect.

To correct the linearity for "Upper expansion and lower compression", the output voltage from pin 2 of Q301 is divided by R308 and R309. This voltage is applied through R352 and R311, to pin 1 of Q501. That is, the sawtooth current component is included in the discharge current from C301 (Reference Sawtooth Voltage Generating Circuit). By applying the sawtooth voltage component to C301, it generates a parabolic component voltage at both ends which acts to compensate for the parabolic component that is fed back to pin 2 of Q501 and thereby compressing the upper part and expanding the lower part of the signal.

For the following components refer to the schematic diagram:

R351 is the linearity adjustment, it will vary the size of the sawtooth waveform to be applied to pin 1 of Q501. By varying R351 the Vertical Linearity is adjusted. R315 and C309 are used to help prevent expansion of the top portion. C311 and C314 are used for phase correction to prevent parasitic oscillations. R336, is the deflection yoke damping resistor. D303 is a special temperature compensating diode used to prevent vertical amplitude drift. R352 is the height adjustment.

VERTICAL CORRECTION CIRCUIT

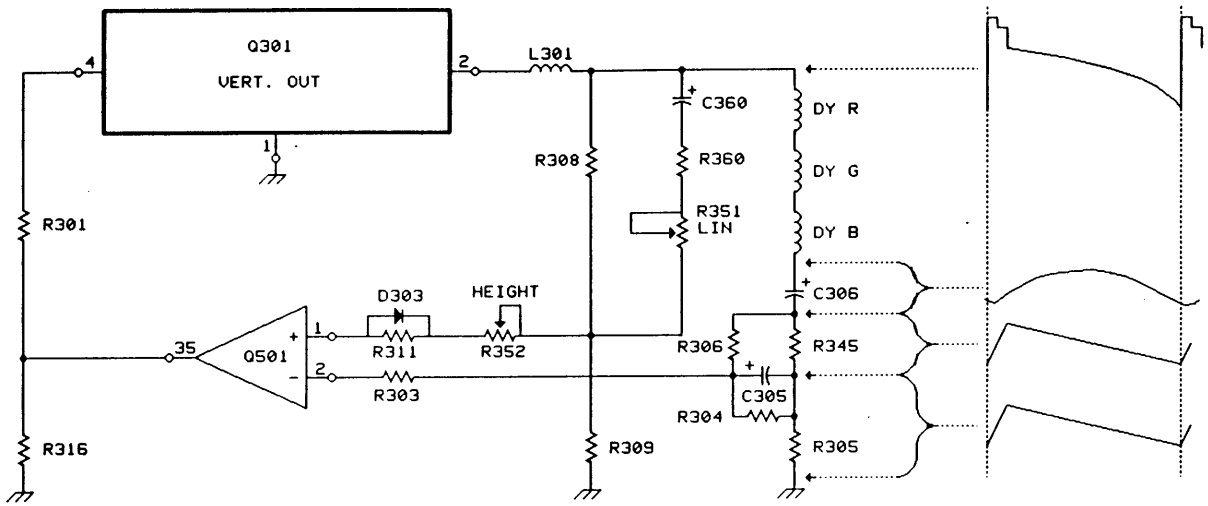


FIG. 5

VERTICAL DEFLECTION CIRCUIT (CONT.)

PROTECTION CIRCUIT

If the deflection current is lost to the deflection coils only a horizontal line will appear on the TV screen. On a projection CRT, because there is no shadow mask, all of the electron beam will be concentrated on the fluorescent screen and it will be burned in a very short time. To prevent this whenever the loss of vertical deflection is detected, the video signal will be blanked thereby cutting off the electron beam in the CRTs. See Figure 6.

THEORY OF OPERATION

During normal operation of the vertical deflection circuit, a sawtooth voltage is obtained at the junction of C306 and R345, this will repeatedly turn Q340 ON/OFF at the vertical rate. The collector voltage of Q340 is filtered by C340 into a DC supply that keeps Q341 and Q342 turned "ON". As a result diode D340 is placed in the cut-off state and has no effect on the Video Blanking operation.

If Vertical Deflection is lost, no voltage will be developed at the connecting point of C306 and R345, this will keep Q340 "OFF" which in turn keeps Q341 and Q342 "OFF". Now this allows the 33V supply from the Audio Circuit to be coupled through R343 and D340 to the Video Out Circuit to cut-off the CRT's.

VERTICAL PROTECTION CIRCUIT

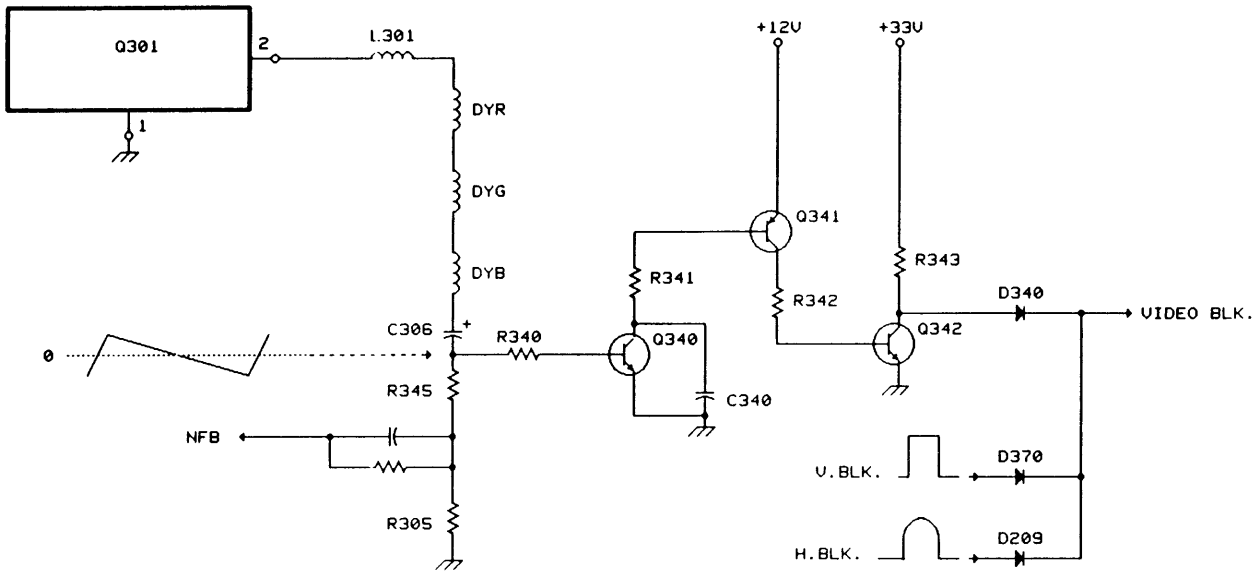


FIG. 6

NOTES

X.

HORIZONTAL DEFLECTION

THE HORIZONTAL DEFLECTION CIRCUIT

The purpose of the Horizontal Deflection Circuit is to supply a 15.734 KHz sawtooth waveform current to the Horizontal Deflection Coil. This will deflect the CRT's electron beam from left to right and provides horizontal deflection on the screen. The Horizontal Deflection Circuit is made up of three sections; The Horizontal Start-up Circuit, The Horizontal Drive Circuit, and The Horizontal Output Circuit. Other sub-circuits include the Horizontal Amplitude and the Linearity Correction Circuits.

The Horizontal Deflection Circuit uses the same configuration as that of the X-63G Chassis. Major differences from the X-63G are as follow:

(1) Three deflection coils are provided as three projection CRT's are equipped. The three deflection coils are connected in parallel so that each is supplied with the same deflection current. Vertical deflection coils are connected in series.

(2) The High-voltage Circuit and the Horizontal Output Circuit are separate systems and therefore the horizontal output transformer is electrically a conventional FBT minus the high-voltage winding.

(3) Horizontal amplitude is adjusted by the Horizontal Width Adjustment Coil. Because left and right pin-cushion distortions are corrected by the Convergence Circuit there is no need for a Pin-cushion Correction Circuit.

(4) The power circuit systems that are taken from the Horizontal Output Circuit have been increased to cope with new circuits such as; the Carver Sound, PIP, Convergence, Electromagnetic Focusing, etc. Power supplies of -12V and -9V are provided, and additonally, the output capacity of the +12V supply has increased.

HORIZONTAL DEFLECTION CIRCUIT

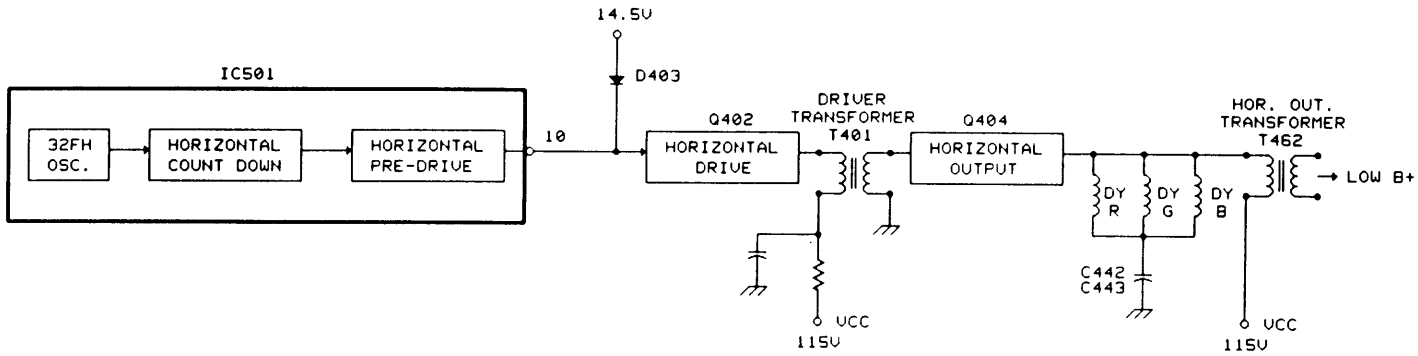


FIG. 1

HORIZONTAL START-UP CIRCUIT

When the Power Switch is turned ON, the Horizontal Start-up Circuit comes on momentarily. The Horizontal Start-up Circuit is the circuit that "initiates" the Horizontal Output Circuit by biasing pin 9 (power source for the Horizontal Oscillator and Pre-driver) of IC 501 and the base of Q402 (Horizontal Drive Transistor).

THEORY OF OPERATION

When the power switch is turned ON (See Figure 2A), the Main B+ Line (115V) and the Audio Output B+ Line (33V) rise at the same time. The 115V line is applied to the base of Q400 through a voltage divider made up of R414 and R442. This turns Q400 "ON". When Q400 turns ON, current flows from the Audio Output B+ Line, through R412, Q400, and D404 so that 8V will develop at point (A). This voltage is applied to pin 9 (H.VCC) of IC 501 through R413, and activates the Horizontal Oscillator and Pre-driver inside Q501. Meanwhile, base current flows from Point (A) through R440 & R411, to the base of horizontal drive transistor Q402, starting the horizontal drive circuit. This is the "Power ON Period" for the circuit inside Q501, the Horizontal Drive Circuit, and the Horizontal Output Circuit.

As the Horizontal Output Circuit rises towards a "Steady State" (See Figure 2B), the 14.5V line voltage which is obtained by rectifying the voltage from pin 12 of the FBT also rises. When the 14.5V line rises and exceeds the voltage at Point "A", D403 turns "ON". This voltage [14.5V] now provides the bias to pin 9 of IC501 and to the base of Q402. Under this condition, D404 and Q400 are turned "OFF" and the power from the Audio Output Power Line is cut off. In this way, by supplying the power from the Audio Out B+ to IC501 and Q402 during the "Power ON Period" and then switching to the 14.5V Line in the "Steady State" to keep the Horizontal Deflection Circuit "On", power consumption in the "Steady State" is reduced to 0.39 Watts as opposed to a conventional circuit where power consumption is 3.9 Watts. Utilizing this system results in a power reduction of 90%.

HORIZONTAL START-UP CIRCUIT

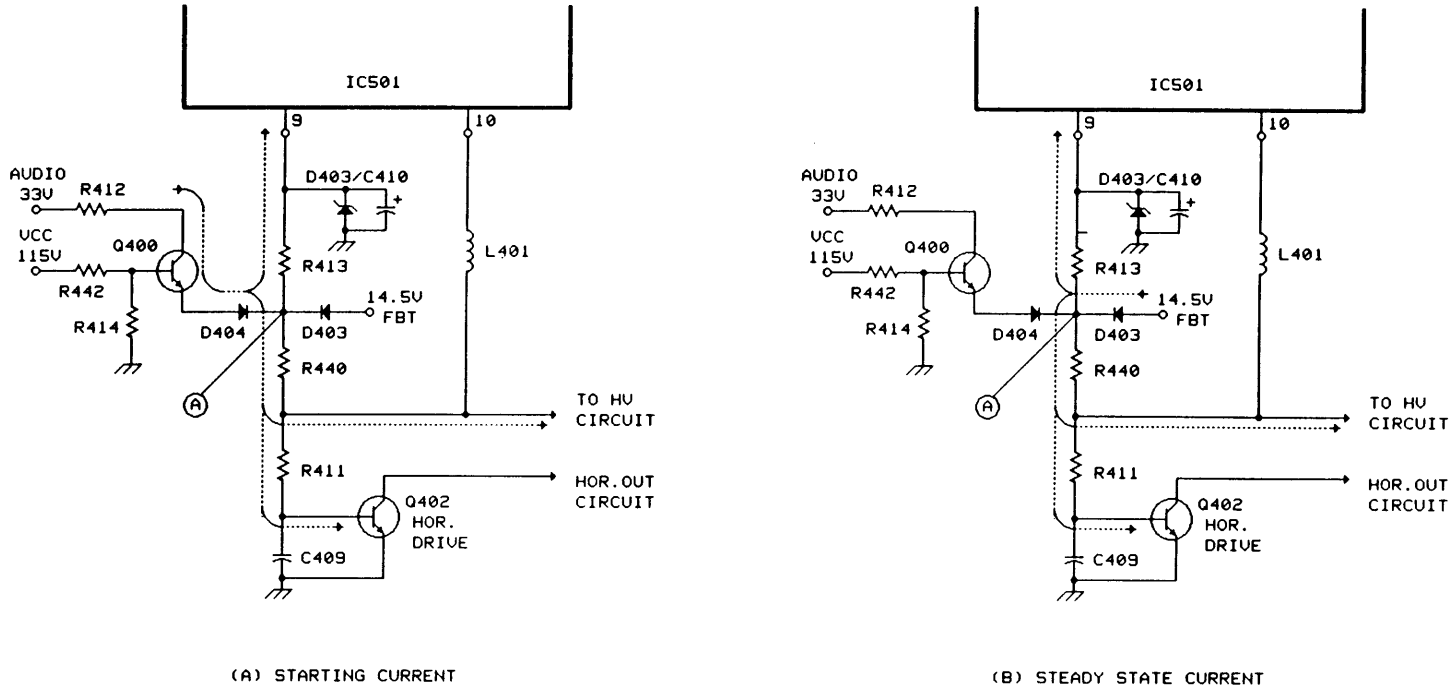


FIG. 2

HORIZONTAL DRIVE CIRCUIT

A heavy base current (IB) must flow into the Horizontal Output Transistor in order for it to rapidly reach its saturation point or its cut-off condition. For this purpose, a Drive Amplifier is provided between the Oscillator Circuit and the Output Circuit to amplify the current to several amperes and to waveshape the pulse voltage, thereby stabilizing the operation of the output transistor.

THEORY OF OPERATION

The Horizontal Drive Circuit works like a switching circuit which applies a pulse voltage to the Output Transistor Base, turning the transistor "ON" when the voltage swing is in the positive direction and turning the transistor "OFF" when the voltage swing is in the negative direction. To completely **turn on** the Output Transistor and make the internal impedance low, a high forward drive voltage must be applied to the base. On the other hand, to completely **turn off** the transistor, a high reverse voltage must be applied to the base. When the Output Transistor is turned "ON", it conducts at the saturation point preventing the transistor from turning "OFF" immediately. Even if a reverse base bias is applied to the base, because of minority carriers stored in the base, it can not be reduced to zero instantly. The time lag required for the base current to disappear is called the **storage time** and **falling time**. (See Figure 3A). To shorten the storage time and the falling time, a sufficiently high reverse bias voltage must be applied to the base before heavy reverse current can flow. This operation also stabilizes the Output Transistor.

The Horizontal Drive Circuit used is called the **Off Drive System,** meaning that when the Drive Transistor is ON, the Horizontal Output Transistor is OFF. (See Figure 3B). The advantages of this circuit are: The energy balance between the ON & OFF periods of the drive circuit is stable and the circuit can be simplified. Also the reverse base current of the Horizontal Output Transistor can be controlled easily. The disadvantage of this circuit is that the base-emitter forward current flowing into the Horizontal Output Transistor is susceptible to on-period variations of the Drive Transistor.

HORIZONTAL DRIVE CIRCUIT

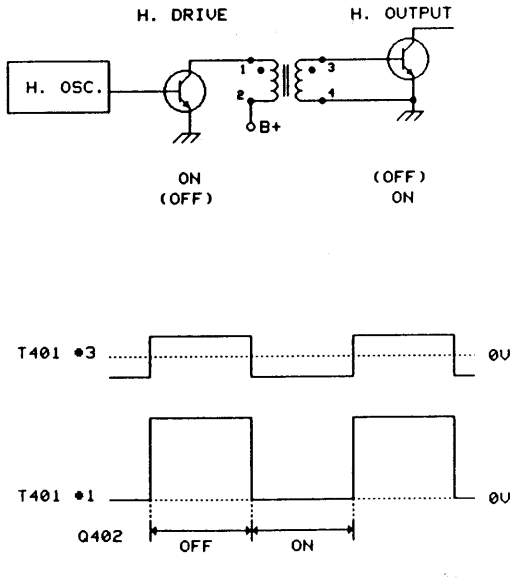


FIG. A

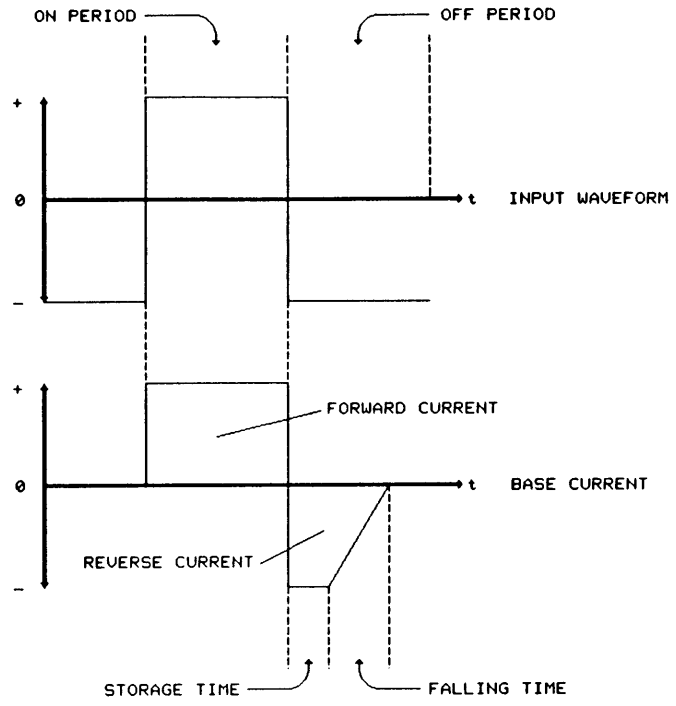


FIG. B

FIG. 3

HORIZONTAL DRIVE CIRCUIT (CONT.)

The Off Drive System Circuit description is as follows. (See Figure 4).

Transistor Q1 (pin 10 of Q501) is repeatedly turned ON/OFF at the horizontal rate. A square wave with a DC voltage of 14.5V is developed by coupling pin 10 of Q501 through L401.

When pin 10 of Q501 is high (Q1 inside Q501 is OFF), a base current flows from the 14.5V supply to the base of Q402 through R440 and R411. The collector current flows from the 115V supply through R416, R417, and T401 to the collector of Q402. The voltage at pins 1 and 2 of T401 should read close to 0V. At this time the Horizontal Output Transistor Q404 does not turn "ON" because the **Off Drive System** is employed. That is, its base-emitter is biased in the reverse direction. On the other hand, when pin 10 of Q501 is 0V (Q1 inside Q501 is ON), Q402 will turn "OFF". The collector of Q402 goes high causing a voltage to develop at the primary winding of the Driver Transformer. This voltage is stepped down and applied to the base of Q404, thereby supplying a high base current that turns "ON" Q404 very rapidly.

The turn ratio between the primary and secondary windings of the driver transformer is 30:1. This means that the pulse voltage being applied to the base of Q404 is greatly stepped down. However, as energy transfer is constant, this will supply sufficient base current to Q404.

HORIZONTAL DRIVE CIRCUIT

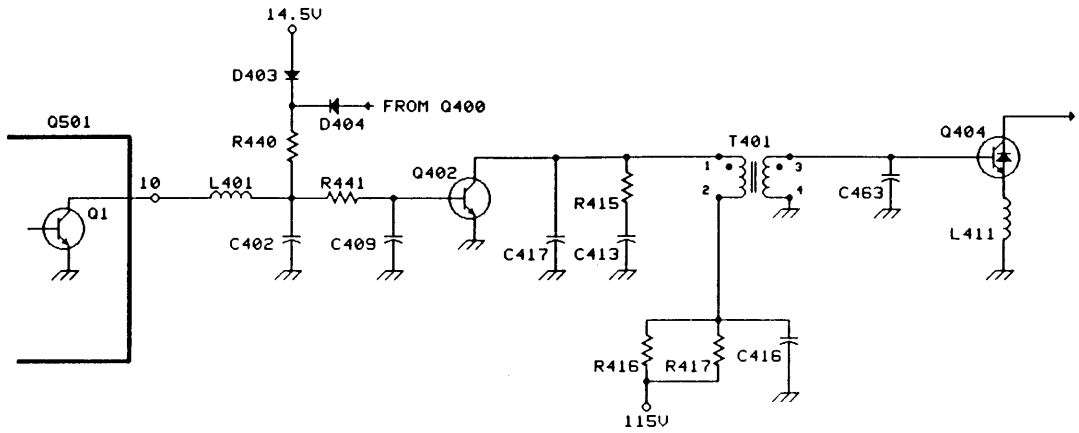


FIG. 4

THE HORIZONTAL OUTPUT CIRCUIT

To perform the horizontal scanning, the Horizontal Output Circuit must apply a 15.734KHz sawtooth wave current to the horizontal deflection coils. The circuit performs this through mutual action of the Horizontal Output Transistor and the Damper Diode (Q404). This deflects the electron beam of all three CRT's from left to right in the horizontal direction.

Basically, during the Horizontal Deflection Scanning (See Figure 5), current flowing through the Damper Diode scans the left half of the screen, after which the current developed by the Horizontal Output Transistor scans the right half of the screen. During the flyback period, both the Damper Diode and the Horizontal Output Transistor are cut off and the oscillation current of the tank circuit (resonant capacitor & deflection coil) is used.

Also, by rectifying pulse voltages tapped from different terminals of the output transformer (T462), low DC voltages can be obtained to power other circuits.

HORIZONTAL OUTPUT CIRCUIT

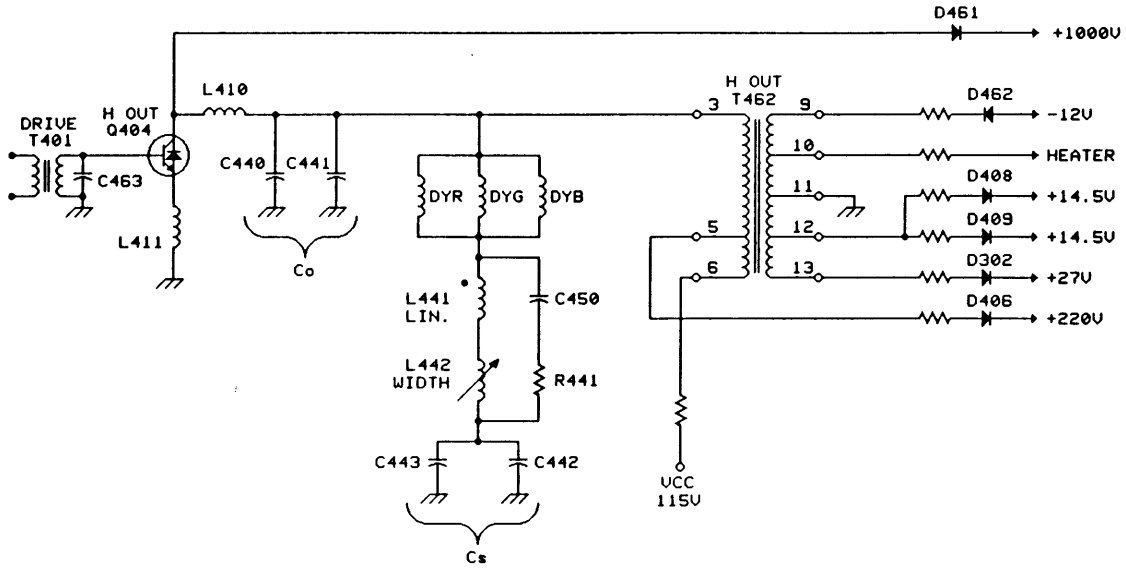


FIG. 5

HORIZONTAL OUTPUT CIRCUIT (con't)

The following is a description of the Timing Chart as it applies to the basic circuit.

A positive pulse from the Hor. Drive Circuit is applied to the base of the Hor. Output Transistor and begins driving it into conduction. The collector current increases from zero at T1 to maximum (Q404 nearly saturated) at T2. This rising current flowing E to C and through the horizontal deflection coils builds up a magnetic field around the coils which scans the electron beam from the center to the right side of the screen. (T1 - T2)

When the drive signal on the base of Q404 drops to zero, the transistor cuts off. This causes the magnetic field build up around the deflection coils to collapse whereby changing direction and horizontal retrace will begin. The energy in the deflection coils is transferred to C440 & C441 during the first half of retrace. The electron beam is now back to the center of the screen. (T2 - T3)

With all of the energy now coupled out of the deflection coils, C440 & C441 begin to discharge through the coils in the opposite direction and continue the retrace to the left side of the screen. When C440 & C441 have fully discharged through the deflection coils, the reverse current will have reached maximum and the electron beam will have reached the far left side of the screen. (T3 - T4)

The collapsing magnetic field caused by a lack of further increasing current flow, will now change the direction of current in the coils and will forward bias the Damper Diode thus coupling the energy out of the deflection coils and moving the electron beam from the left side of the screen back to the center. (T4 - T6)

At this point in time, the Drive Signal from the Horizontal Drive Circuit is applied to the base of Q404 to repeat the cycle. (T1 - T2)

HORIZONTAL OUTPUT CIRCUIT

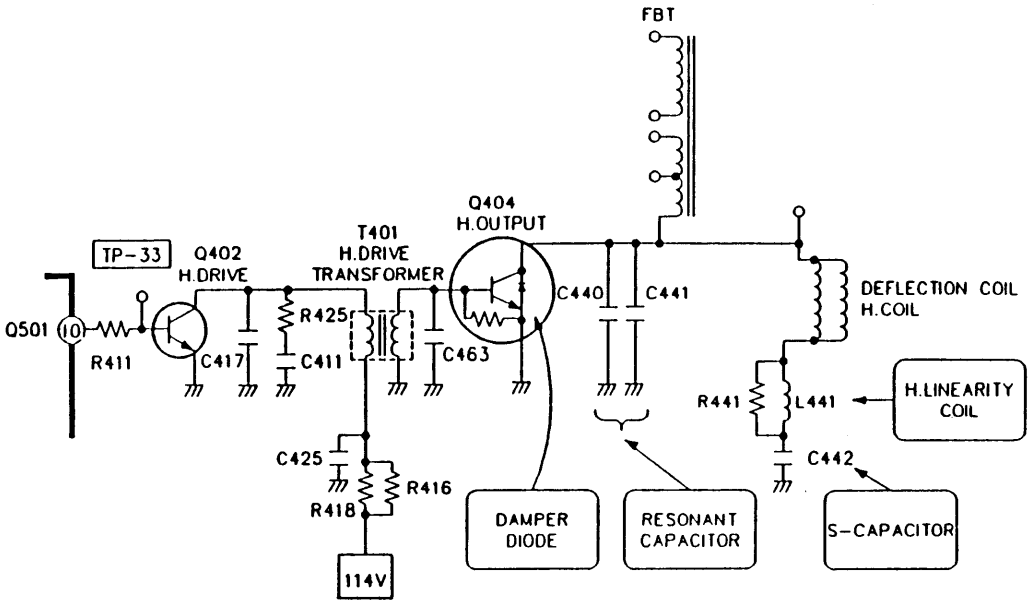


FIG. 6

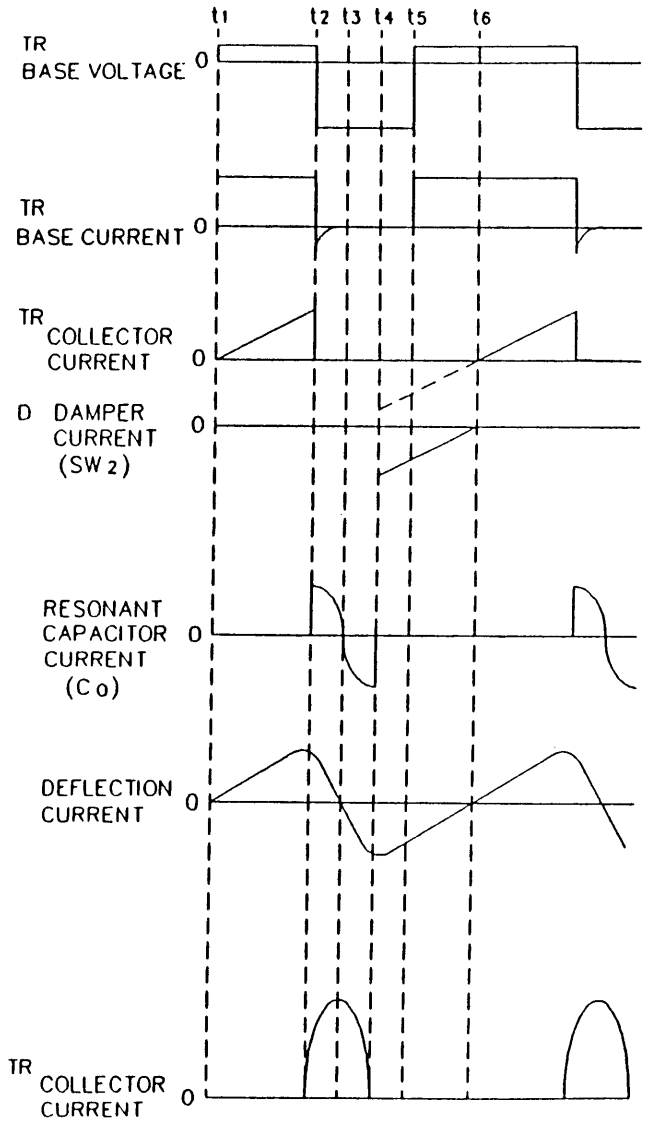


FIG. 7

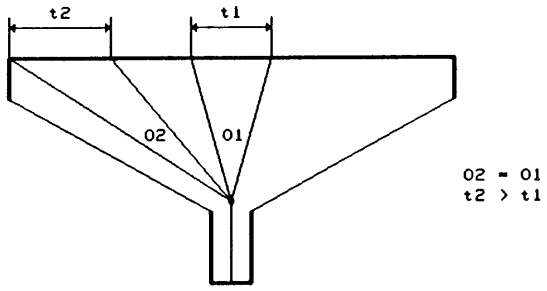
LINEARITY CORRECTION

S-CURVE CORRECTION (S CAPACITOR)

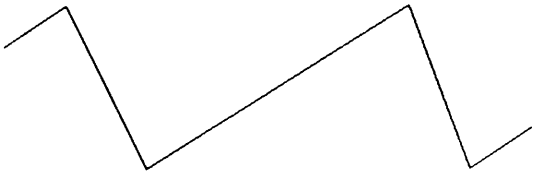
If a sawtooth current with normal linearity flows into the deflection coil, when the deflection angle at the picture tube increases, the picture will be expanded at the left and right ends of the screen. This is because at the same projected angle (0) the image size on the center of the screen will cover a smaller area than the image size at the circumference of the screen. To suppress this expansion at the screen circumference, it is necessary to set the deflection angle (0) to a larger value (the electron beam will be deflected faster) at the screen's center area, and set the deflection angle (0) to a smaller value (the electron beam will be deflected slower) at the circumference area, see Figures 8 A&B. Elongation at the peripheral area of the screen can be corrected by suppressing elongation of the deflection current corresponding to the peripheral area of the screen. This suppression is realized by **superposing** an S-waveform current to the sawtooth current. To accomplish this operation, S-capacitors C442/C443 (CS) are connected in series to the deflection coils. See Fig. 9A.

In the horizontal output circuit shown in Figure 9A the capacitor CS is connected in series with the deflection coil L to block DC current. By properly selecting the value of CS so that it constitutes a resonant circuit with the deflection coil's inductance LH, a sinewave current as shown in Figure 9C will be obtained. When the sinewave current is superimposed on the sawtooth current shown in Figure 9B, a current as shown in Figure 9D will be obtained. In this manner an S-curve current flowing into the deflection coil will produce the **slow scanning at the left & right edge of the screen**, and the **fast scanning in the center area of the screen** that is necessary for producing a picture with good linearity.

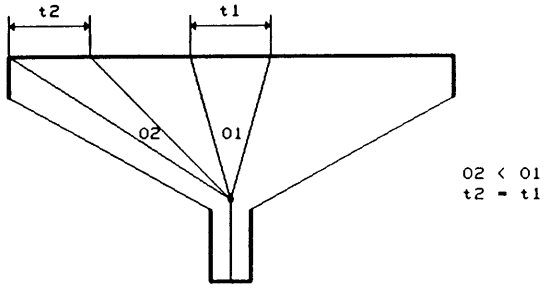
LINEARITY CORRECTION



02 = 01
t2 > t1



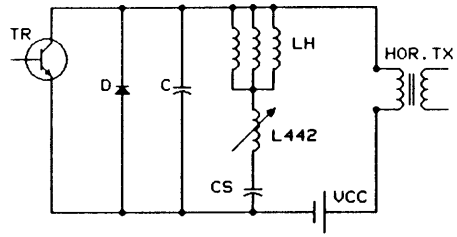
(A) NORMAL



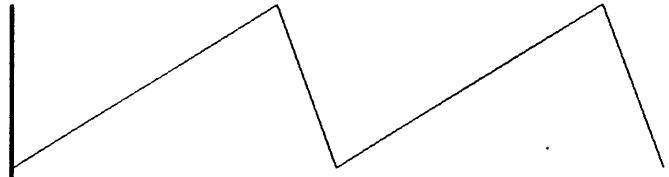
02 < 01
t2 = t1

(B) S-CORRECTION

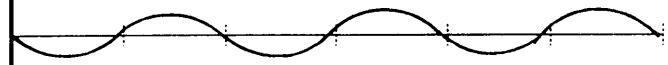
FIG. 8



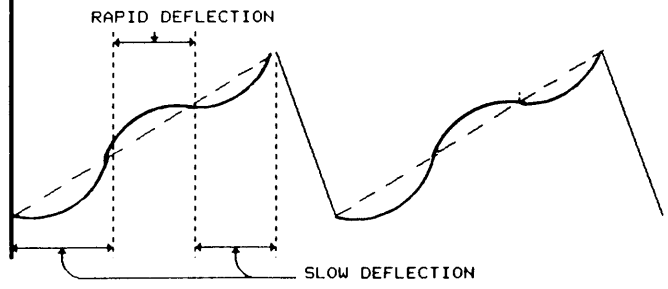
(A) H. OUTPUT CIR.



(B) SAWTOOTH WAVE CURRENT



(C) RESONANT CURRENT (CS/LH)



(D) COMBINED CURRENT

FIG. 9

LINEARITY CORRECTION (CONT.)

HORIZONTAL AMPLITUDE ADJUSTMENT

To change the horizontal amplitude, it is only necessary to change the size of the sawtooth current flowing through the horizontal deflection coils. Therefore the horizontal amplitude is adjusted by changing the inductance of the Width Adjustment Coil (L442) which is connected in series with the Horizontal Deflection Coils. See Fig. 10.

LEFT-RIGHT ASYMMETRICAL CORRECTION (LIN. COIL)

In the circuit shown in Figure 10, the Deflection Coil Current (IH) does not flow straight as shown by the dotted line in Figure 11A, but instead flows as shown by the solid line. This effect is due to the characteristic of the Damper Diode during the first half period of scanning (left side of screen), and the effect of resistance of the Deflection Coil during the second half period of scanning (right side of screen). Because of this, the deflection current becomes a sawtooth current with inadequate linearity, resulting in the reproduction of an asymmetrical picture at the left and right sides of the screen (left side expanded, right side compressed).

To correct this distortion, it's desirable to have a linearity coil having an inductance characteristic that becomes larger for Negative Deflection Current (deflection current flowing through the damper diode), and then becomes smaller for positive deflection current (deflection current flowing through the output transistor) connected to the deflection coils in series. This characteristic is decided by the size of the ferrite core, the magnetic force of the magnet, the number of turns of the winding, etc. and it's designed to provide the best linearity on the screen.

When a Horizontal Linearity Coil (L441) with a current characteristic as shown in Figure 11B is used, this makes the inductance high at the left side of the screen and low at the right side of the screen, this in turn will compress the left side of the picture and expand the right side of the picture. In this manner, the left-right asymmetrical correction is carried out and the results is a picture with good linearity. Therefore, the Deflection Coil Current (IH) now flows straight as shown by the doted line in Figure 11A.

LINEARITY CORRECTION

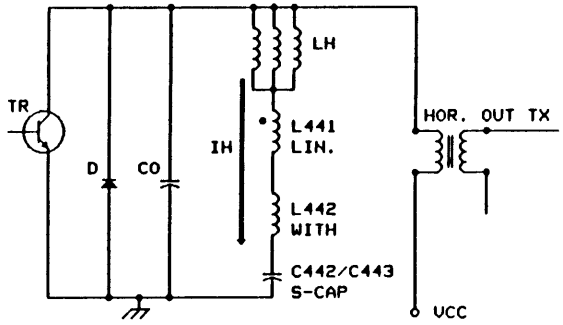
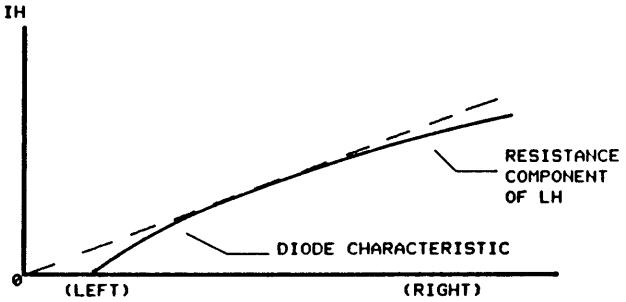
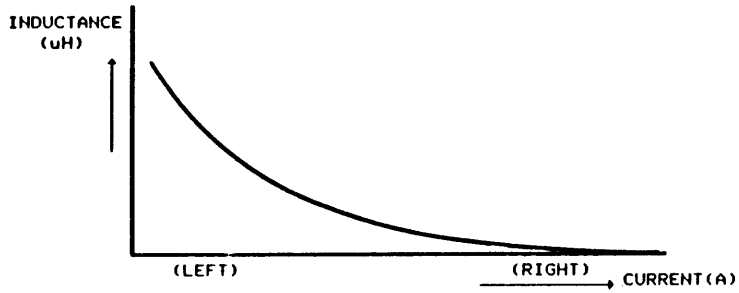


FIG. 10



(A) DEFECTION COIL CURRENT



(B) LIN COIL CHARACTERISTICS

FIG. 11

LOW VOLTAGE GENERATION CIRCUITS

Because the high voltage power is generated in another separate circuit (in the Power PCB), T462 is used to produce low-voltage power only. These voltages are supplied to the following circuits:

(1) Power source for screen electrodes; Approx. 1000Vpp horizontal flyback pulse is obtained at the primary winding of T462 Pin 3. This pulse is rectified and filtered by D461/C465 to +1000V. This is the screen voltage supply to the CRT Drive PCBs.

(2) Power source for the Video Output Circuit; A positive flyback pulse voltage is obtained at the primary winding Pin 5. This pulse is rectified and filtered by D406/C447, the output is stacked with the +115V main power supply and a +220V source is achieved. This is the power supply to the Video Output Circuit of the CRT Drive PCBs.

(3) Power source for the vertical output circuit; A negative Flyback pulse during the scanning period is obtained from the secondary winding Pin 13. This pulse is rectified and filtered by D302/C361 to +27V. This voltage (VCC) is supplied to pin 7 of the Vertical Output IC (Q301).

(4) Heater voltage for the CRTs; A pulse voltage is obtained from the secondary winding Pin 10 and remains unrectified. This pulse is supplied as AC voltage to the heater electrodes of the projection CRTs. The voltage is regulated by R469 so that the heater voltage remains at 6.3V rms.

(5) The +14.5V power source, (2 circuits); In the first circuit, a negative retrace pulse during the scanning period is obtained from the secondary winding Pin 12. This pulse is rectified and filtered by D408/C449 and regulated by Q181 so that a +12V source is achieved. In the second circuit, the same pulse is also rectified and filtered by D409/C446 to +14.5V. This voltage is supplied to the Convergence and Focus Circuits. This same voltage is also regulated by Q182 so that a +9V source is achieved.

(6) The -12V power source; A positive pulse during the scanning period is obtained from the secondary winding Pin 9. This pulse is rectified and filtered by D842/C466 to -12V. This will be supplied to Convergence and Focusing Circuits. Also, this voltage is regulated by Q490 so that a -9V source is achieved.

LOW VOLTAGE GENERATION CIRCUIT

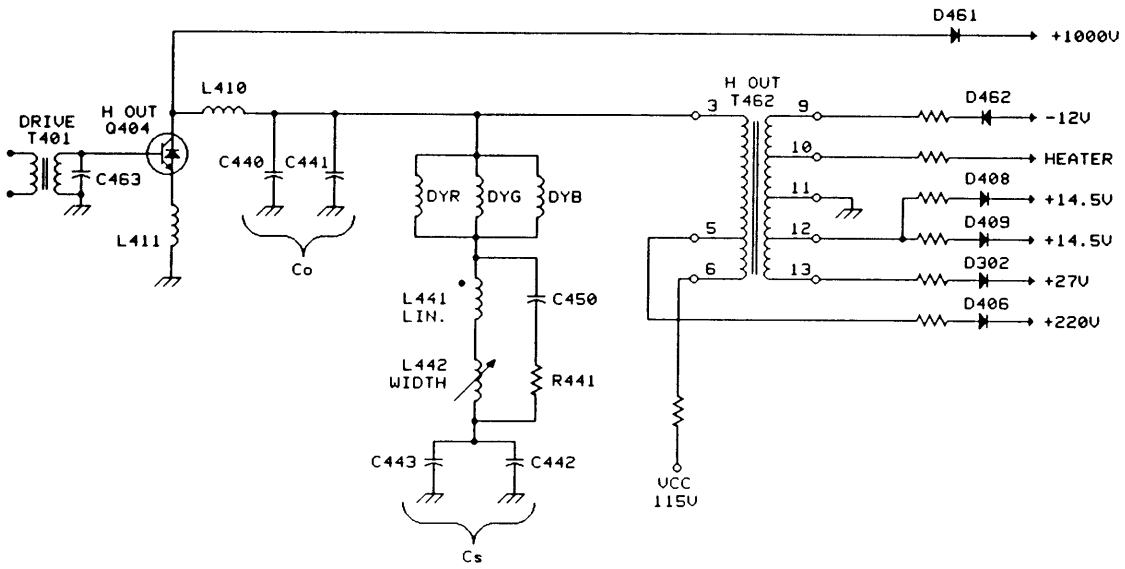


FIG. 5

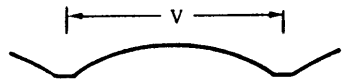
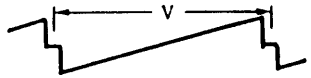
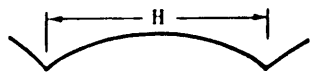
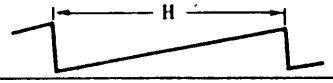
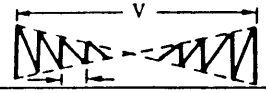
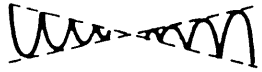
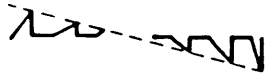
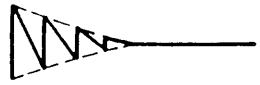
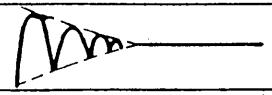
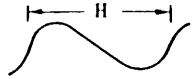
CONVERGENCE CIRCUIT

This circuit consists of the correction signal generator, the matrix circuit to which the correction signals are applied to, and the output circuit which amplifies the output from the matrix circuit and outputs it to the convergence yoke. The convergence correction signals are produced on the basis of horizontal and vertical retrace pulses. The correction signals are shown in Table 1.

Note:

VP	Vertical parabolic wave
HP	Horizontal parabolic wave
VS	Vertical sawtooth wave
HS	Horizontal S-shaped wave
VSHS	Vertical, horizontal sawtooth waves
VSHP	Vertical, sawtooth wave, horizontal parabolic wave
VSHSH	Vertical sawtooth wave (horizontal sawtooth wave 1/2)
HS	Horizontal sawtooth wave

TABLE 1

	Name	Waveform	Movement of Raster
1	VP		Correction of vertical linear distortion Correction of horizontal arched distortion
2	VS		Correction of vertical amplitude distortion Correction of horizontal tilt distortion
3	HP		Correction of vertical arched distortion Correction of horizontal linear distortion
4	HS		Correction of vertical tilt distortion Correction of horizontal amplitude distortion
5	VSHS		Correction of vertical trapezoidal distortion Correction of horizontal trapezoidal distortion
6	VSHP		Correction of vertical pin-cushion distortion
7	VPHS		Correction of horizontal pin-cushion distortion
8	VSHSH		Correction of horizontal left trapezoidal distortion
9	VSHHS		Correction of vertical upper trapezoidal distortion
10	VPHHS		Correction of horizontal left pin-cushion distortion
11	VSHHP		Correction of vertical upper pin-cushion distortion
12	C-KEY		Correction of vertical peripheral trapezoidal distortion
13	HS		Correction of horizontal S distortion

CONVERGENCE CIRCUIT (Cont)

SIGNAL GENERATING CIRCUIT

No. 1 - No. 9 Signals shown in Table 1 are obtained from the input of horizontal and vertical flyback pulses to IC QJ01. A sawtooth wave is produced from the fact that when a capacitor is charged with constant current, voltage at both ends rises linearly with the lapse of time. A horizontal sawtooth wave is obtained when CJ10 is charged with constant voltage and discharged during the horizontal flyback period. A vertical sawtooth wave is obtained in a similar manner by charging CJ03 with a constant current. Parabolic waves are obtained by integrating the above-mentioned waveforms. Horizontal parabolic waves are obtained through integration by RJ09, CJ08 and the operational amplifier in the IC. Vertical parabolic waves are obtained through integration by RJ08, CJ05 and the operational amplifier in the IC. Such modulated correcting waveforms as vertical sawtooth wave, horizontal sawtooth wave, etc. are obtained by processing the above-mentioned 4 types of waveforms which become the basis for correcting waveform by the multiplexer (multiplication circuit) housed in the IC. Relation between I/O waveforms of the IC is shown in Fig. 1 & 2.

The No. 10 Signal VPHHS, is obtained by slicing the underside of the signal at Pin #16 of IC QJ01. The underside slicing is performed by op-amp QJ17 Pins 1-3, and DJ10/DJ09.

The No. 11 Signal VSHHP, is obtained by extracting only the first half of the vertical period of the signal at pin 18 of IC QJ01. The waveforms and the circuit diagram are shown in Fig. 2. A vertical sawtooth wave inputs pin #3 of QJ18. QJ18 operates as a zero cross comparator, and at pin #1 the latter half of the vertical period is about +12V. Its output is obtained by extracting the first half of the vertical period of VSHP.

The No. 12 Signal C-KEY is obtained by extracting the high level portion only of VSH by DJ11 and DJ12.

The No. 13 Signal HS, is obtained through Miller integration of the horizontal sawtooth wave by QJ17.

CONVERGENCE SIGNAL GENERATING CIRCUIT

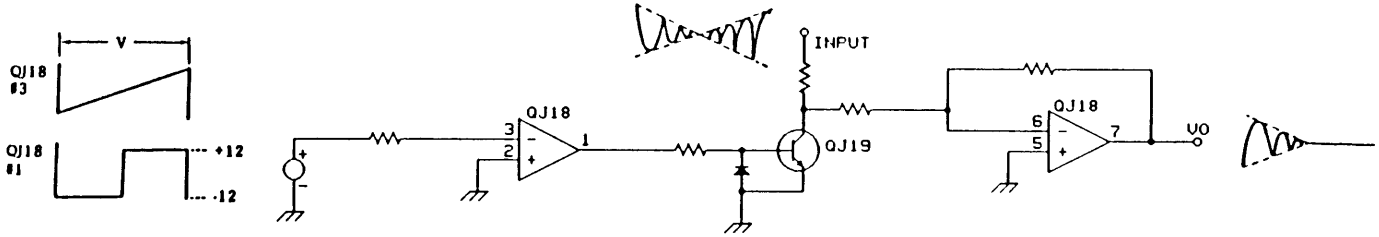


FIG. 1

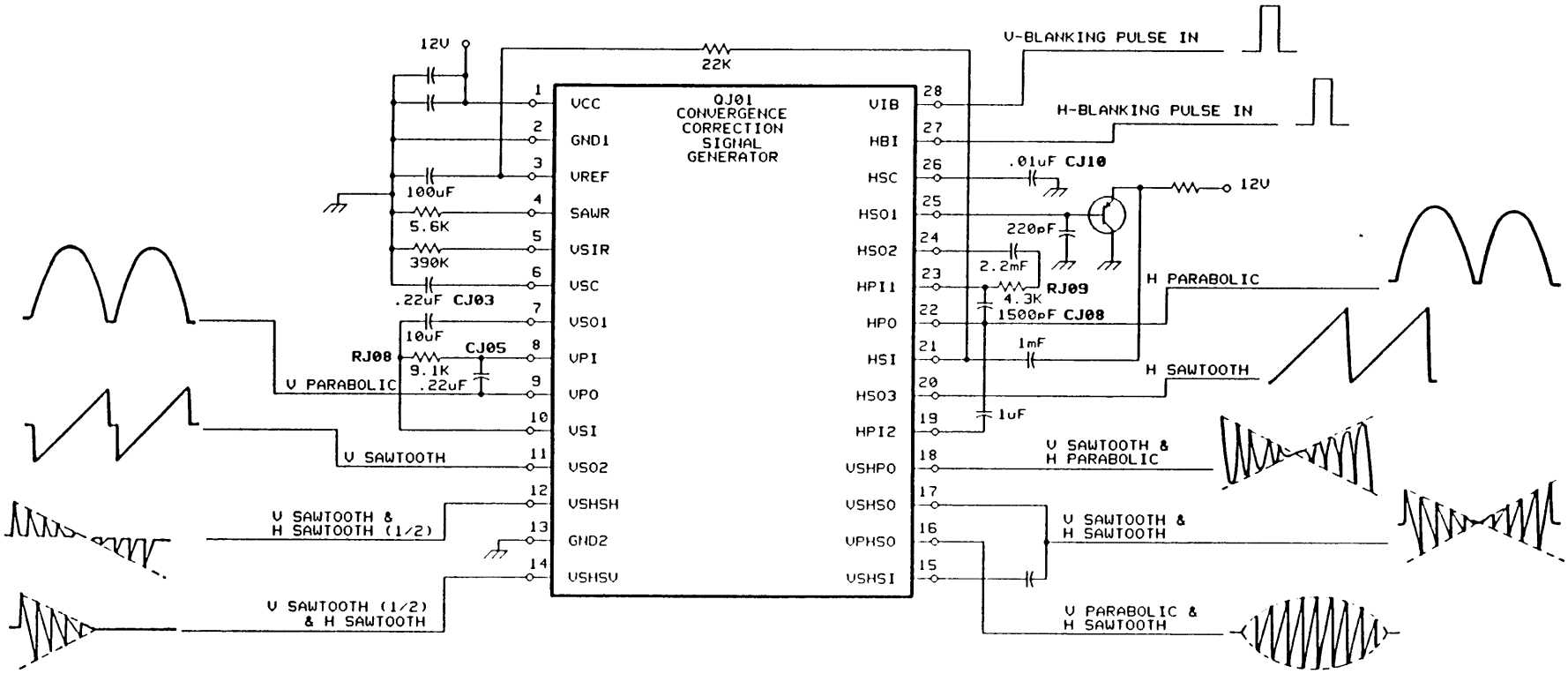


FIG. 2

CONVERGENCE CIRCUIT (Cont)

MATRIX CIRCUIT

The Matrix Circuit is made up of four systems: the vertical circuits for red and blue, and horizontal circuits for red and blue. A matrix circuit is shown in Fig. 3. Q1 and Q2 operate as the current input amplifier. The positive input terminals of Q1 and Q2 are at ground potential, the negative input terminals are set at a zero potential. Both positive and negative outputs are obtained through adjustment of the convergence control.

OUTPUT CIRCUIT

The Convergence Output Circuit is made up of 6 systems; the vertical and horizontal output circuits for red, blue and green, respectively. All circuits are identical to each other therefore only the Red Horizontal Output Circuit will be described here. See Fig. 4.

Q702 is a differential amplifier that operates as a Current Feed-back Amplifier Circuit. It compares the input signal voltage with the feedback voltage through R726 and converts them both into the same waveform. Since current from the convergence coil flows through R726, the current waveform is produced at both ends. That is, the input voltage waveform becomes the same as that of output current (the convergence coil current).

Output from the Differential Amplifier Circuit is supplied to the drive transistor at Q701 (1/2) through the current stabilization circuit of Q702 (1/2). R703 operates as a bootstrap and R706/R707 are load. R703 causes the impedance to become larger and therefore the voltage gain of the drive circuit increases. The push-pull output circuit composing of Q703 through Q706 is controlled by the drive circuit to supply correction current to the convergence coil. Diodes D701, D702 and D713 give bias to the output stage so that both the NPN and PNP output transistor are not cut-off at the same time

CONVERGENCE MATRIX & OUTPUT CIRCUITS

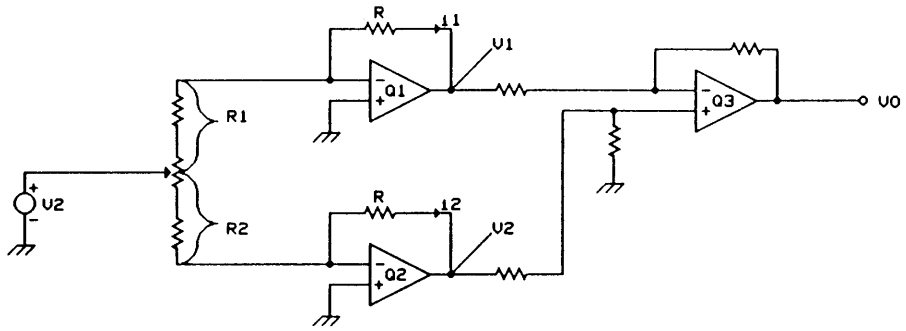


FIG. 3

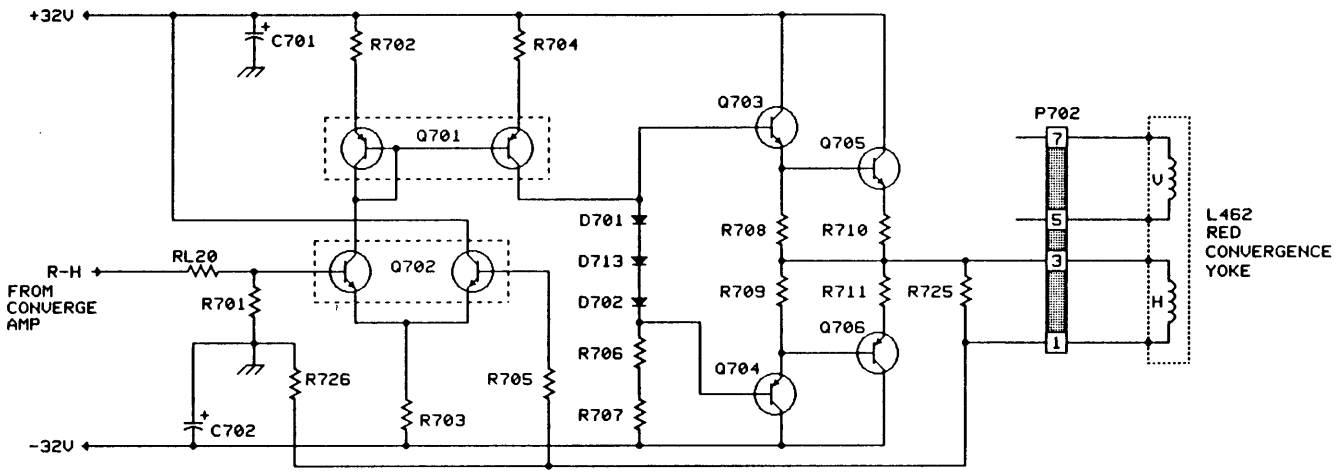


FIG. 4

FOCUS CIRCUIT

This set uses an Electromagnetic Focusing System. The focusing yoke consists of a permanent magnet and a coil for temperature compensation as well as dynamic focusing. It is necessary to supply current for temperature compensation to the coil since the magnetic flux decreases at higher temperatures. The green focusing yoke houses a thermistor for detecting temperature. The set also uses a Dynamic Focusing System in which a parabolic wave at the vertical rate flows through the coil correcting the vertical dynamic focus. The output circuit is available for all three CRTs; red, blue and green. Only the red system is illustrated in Fig. 5.

Description of Circuit Operation

During Electromagnetic Focusing, Q1 and Q2 in the diagram make up a current stabilization circuit. Since R3 = R3S and R5 = R5S, current (I2) flowing to R5 and current (I1) flowing to R3 are equal to each other. The positive input terminal of Q3 is the signal input terminal and the negative input terminal is set at zero reference. To compensate for changes in the magnetic flux during a high temperature state the resistance of the thermistor (RTH) decreases. Current flowing to R3 increases and I1 becomes larger. Since I2 will remain constant regardless of temperature, I3 increases by the increment of I1. The resultant voltage of RF and I3 outputs from terminal V01 of Q3, and will in turn increase the current (IF) flowing to the coil thereby compensating magnetic flux changes of the permanent magnet. In the case of low temperature, a reverse operation is carried out.

During Vertical Dynamic Focusing, a vertical parabolic wave from the Convergence Correction Signal is divided by a resistor network and inputs to the positive terminal of Q3. The output of Q3 is a Dynamic Focus Compensating Current that flows to the coil. Further, since the coil cannot be driven directly by Q3, an output transistor is provided and used as a buffer at the output stage. V01 is applied to the positive input of Q4 and VNF (current flowing to the coil converted to voltage by RK) is fed back to the negative input of Q4, resulting in V01 becoming equal to VNF. Therefore, current (IF) flowing to the coil becomes equal to V01/RK and will not be affected by impedance drift and the like.

STATIC FOCUS CIRCUIT

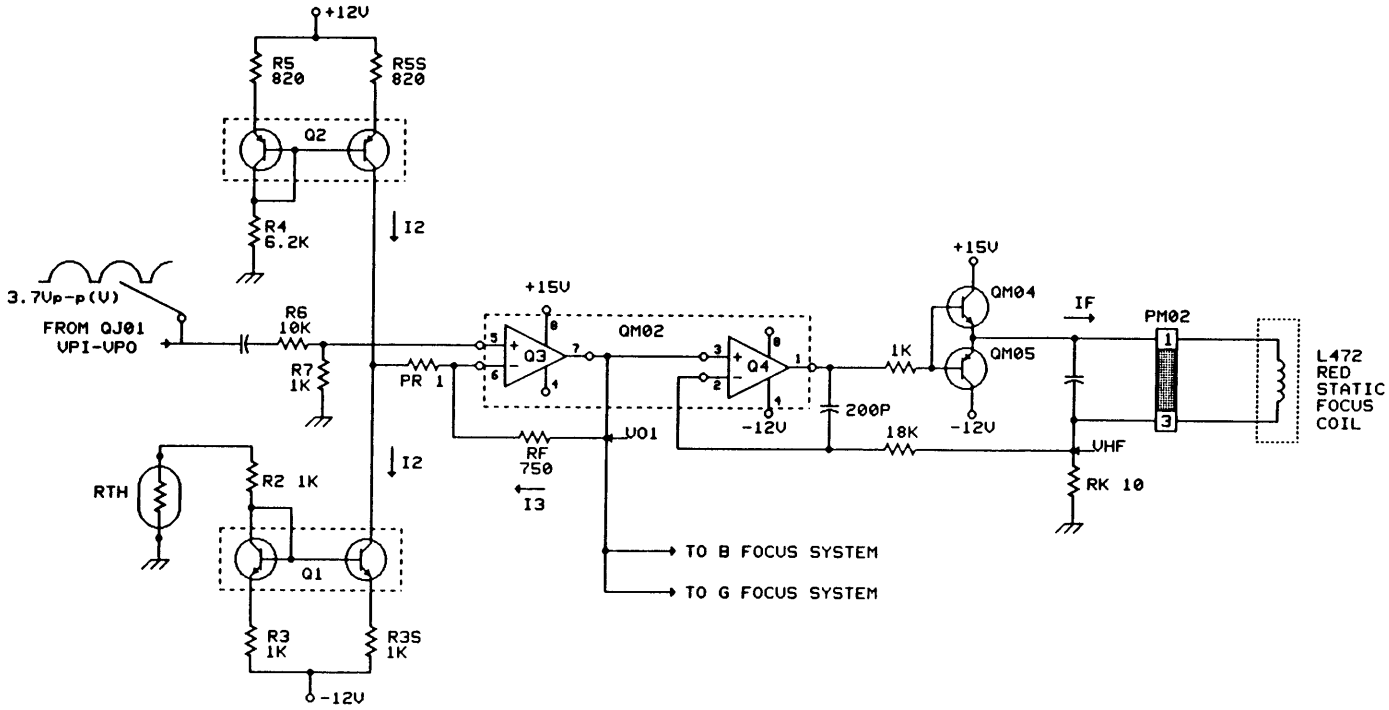


FIG. 5

HIGH-VOLTAGE CIRCUIT

The High-voltage Circuit is used only to supply high-voltage power (31KV) to the anode of the projection tubes. The entire high-voltage circuit consists of a High-voltage Generation Circuit, High-voltage Stabilizing Circuit and the X-ray Protection Circuit. It operates on +115V from the Main Power, +12V from the horizontal output transformer T462 and the horizontal output signal from Q501 Pin 10.

High-Voltage Generating Circuit

Horizontal oscillation pulses are supplied from pin 10 of Q501 to the base of Q420, which performs the switching operation during the horizontal cycle. (Q420 and Q501 are located on the main PCB). The base of Q415 is connected to the collector of Q420 therefore, Q415 also performs the switching operation during the horizontal cycle. The switching circuit, consisting of Q407 and T420, is a high-voltage drive circuit and its operation is identical to that of the horizontal drive circuit. See Fig. 1.

The switching circuit, consisting of Q420 and Q415 is simply a buffer circuit connected between the Hor. Osc. Circuit and the High-voltage Drive Circuit. Insertion of the Buffer Circuit is necessary to prevent picture distortion and jitter that might be generated and passed from the High-voltage Circuit to the Horizontal Deflection Circuit. (Changes in the high-voltage load current are caused by changes on picture patterns).

Because Q408 is a high-tension output transistor and C427, C428 and C432 are resonance capacitors, they make this circuit similar to the Horizontal Output Circuit minus the deflecting coils. And by replacing the pulse transformer with a FBT its operation principle is identical to that of the horizontal output circuit. A pulse of approximately 1000V p-p is obtain at the primary winding of the FBT. It is boosted, rectified and filtered by the FBT and outputs as DC31KV. This HV is supplied to the anodes of all three projection tubes.

The FBT houses a 5500pF filter capacitor that reduces high-voltage ripple resulting from fluctuations of the dynamic load current. A 440M resistor is also housed in the FBT which detects the HV and feeds it back to the high-voltage stabilizing circuit.

HIGH VOLTAGE GENERATING CIRCUIT

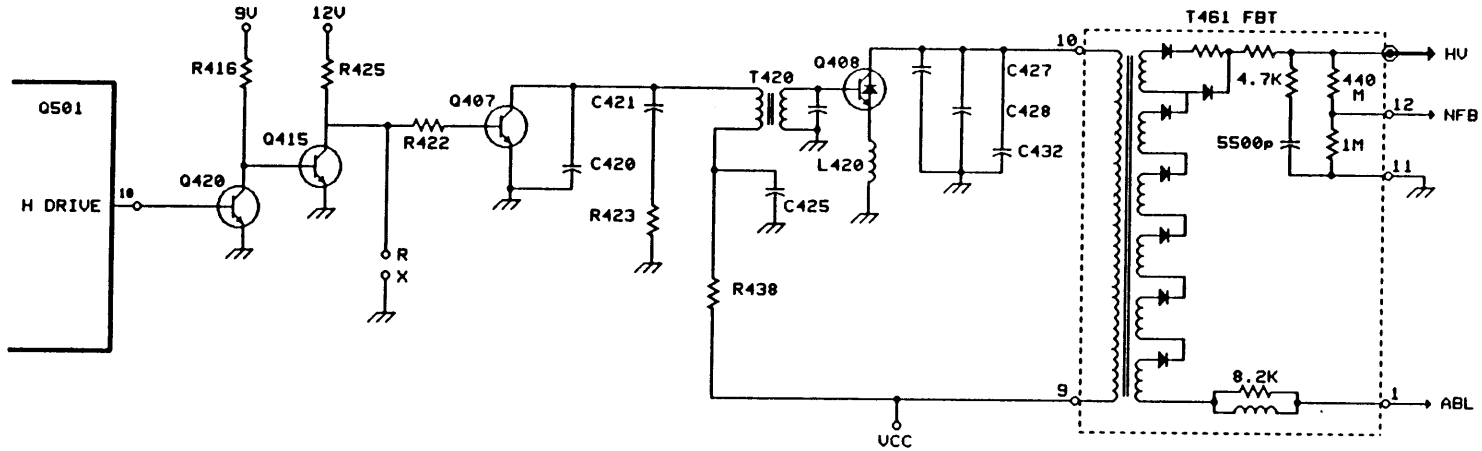


FIG. 1

HIGH-VOLTAGE STABILIZING CIRCUIT

As stated previously, projection televisions have adopted the Electromagnetic Focusing System (magnetic focusing). Here the electron beams are focused by giving them a rotary motion. This is done by applying a parallel magnetic field. This technique is used because it has a far better focusing quality. However because of this focusing system, it is necessary to maintain the anode voltage of the picture tubes at an extremely stable level. Because the anode voltage must remain unchanged, a high-voltage stabilizing circuit is used. See Fig. 2.

IC Q401 contains two operational amplifiers. Voltage detected by the internal resistor of the FBT inputs to the non-inverting input (pin 3) of A1. Since the inverting input (pin 2) and the output terminal (pin 1) of A1 are shorted, A1 operates as a buffer amplifier. The detected voltage outputs pin 1 and is applied to the non-inverting input (pin 5) of A2. A reference voltage is obtained by dividing the 32V zener voltage from D420 through R432, R451 and R433. This reference voltage inputs the inverting input (pin 6) of A2. This reference voltage is compared with the detected high-voltage (pin 5), and an error voltage outputs at pin 7. If the high-voltage drops, for instance, the output voltage of A2 will also drop.

The error amplified signal, outputs Q401, passes through R429 and zener diode D421 for level shifting and is applied to the base of Q405, where it is further amplified.

Q410 is a high-voltage control transistor and Q409 is a driver transistor. They are connected in a Darlington configuration to provide a large current amplification factor. The DC voltage that outputs from the emitter of Q410 is the supply voltage to the previously described high-voltage circuit.

If the high-voltage drops, the voltage at pin 7 of Q401 also drops causing both the base and collector currents of Q405 decrease. As a result, current flowing to R434 and R445 decreases and the base voltage of Q409 rises. Because the circuit consisting of Q409 and Q410 is an emitter follower circuit, the emitter voltage of Q410, (supply voltage to the FBT) also rises pulling the high-voltage up.

HIGH VOLTAGE STABILIZING CIRCUIT

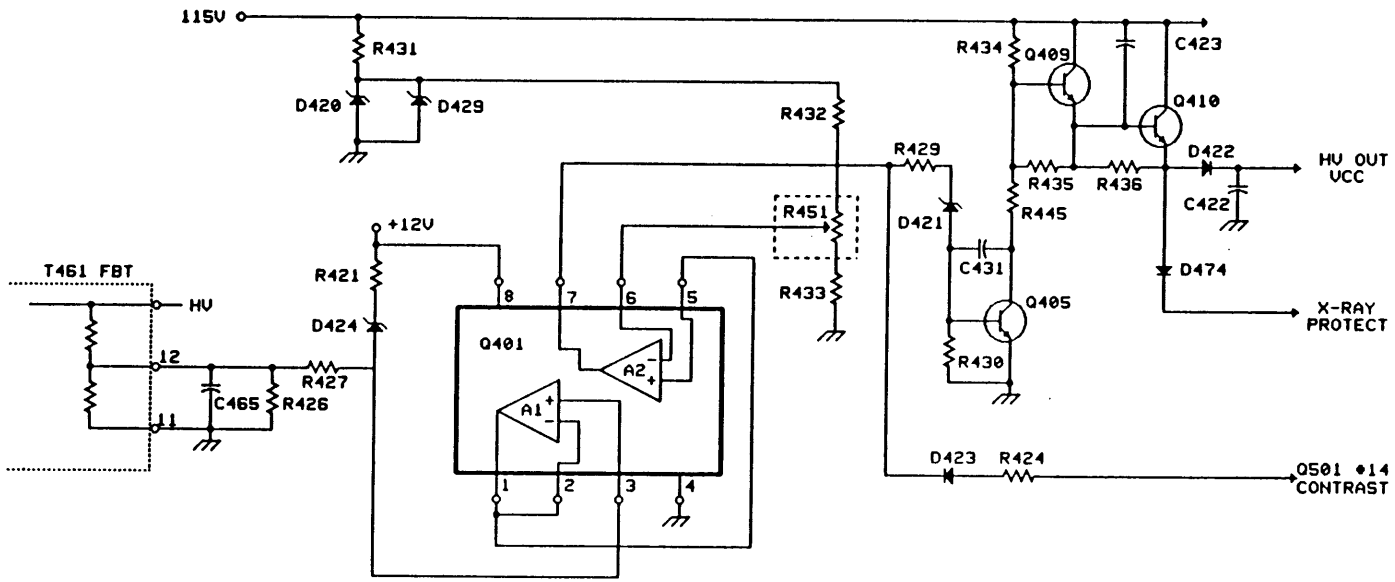


FIG. 2

HIGH-VOLTAGE STAVILIZING CIRCUIT (Cont)

The electrostatic capacitance of the filter cap. C422 must be set at minimum in order for the stabilization circuit to respond faster to high-voltage variations. Because of this, a very large parabolic voltage is generated accross this capacitor and at a period when an instantaneous voltage value that exceeds the emitter voltage of Q410 can be generated. So, to prevent this reverse voltage spike from being applied to the base and emitters of Q410 and Q409, D422 is installed between C422 and Q410.

R451 is a variable resistor that regulates the reference voltage to A2. The resistor controls the supply voltage to the high-voltage output circuit and insures a 31.0 kV output. This variable resistor is designed to be covered by a shielded case after regulation is set to prevent it from being turned unnecessarily. (It is necessary to maintain the correct setting to prevent X-ray radiation).

The reason for providing two zener diodes D420 and D429 on the reference voltage circuit is to prevent an abnormal rise of high-voltage even when one of the zener diodes gets damaged.

Zener diode D424 on the input side of the circuit limits the lower value of the HV detection voltage and prevents latch-up of the operational amplifier by high-voltage spikes.

Diode D423 corrects any response delays of the ABL circuit and controls the voltage at the contrast terminal of Q501 (on the main unit). For instance, if the screen is switched suddenly from a dark picture to a bright picture as a result of channel switching or changes in the broadcast signals, and since the voltage gain of the video amplifier circuit is quite large, a very large anode current will flow and high-voltage will drop abnormally causing the picture to becomes obscure and hard to see. At this time, the voltage at pin 7 of Q401 also drops abnormally, D423 is turned ON to lower the voltage at the contrast terminal (pin 14) of Q501 and suppresses the increase of anode current. The response of this part of the circuit is faster than the response of the ABL circuit, so the anode current is corrected and the picture does not actually become dark. During normal operation D423 is kept OFF and has no effect on the video signal circuit.

HIGH VOLTAGE STABILIZING CIRCUIT

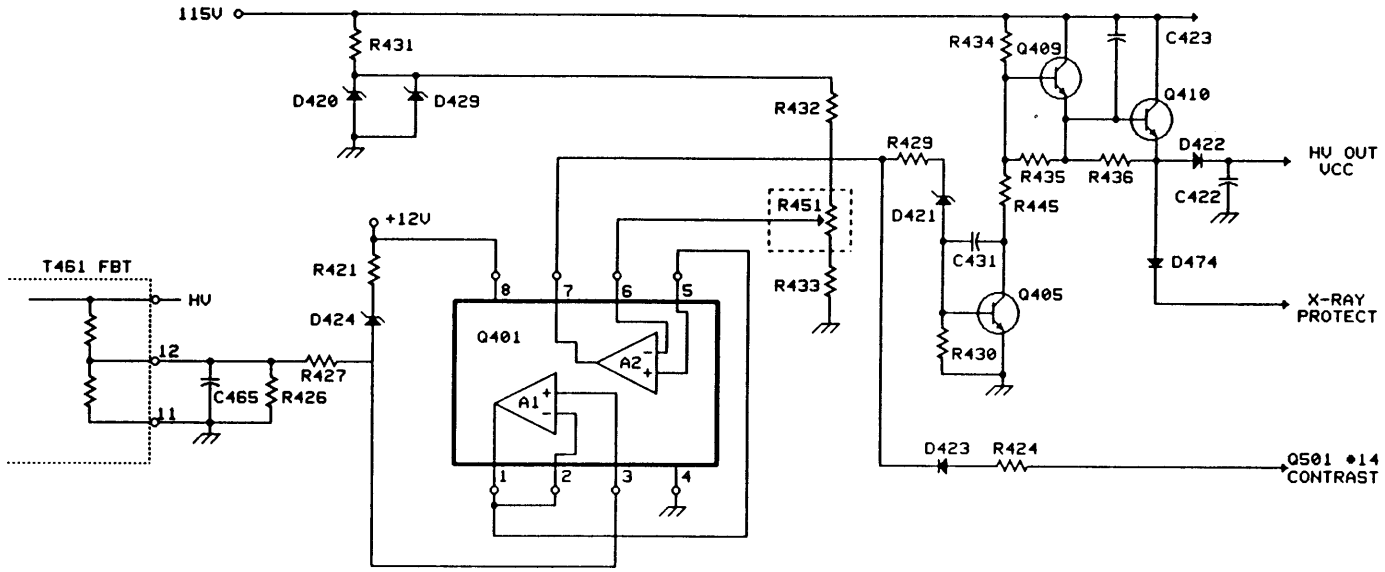


FIG. 2

X-RAY PROTECTION CIRCUIT

X-Rays are produced when high-speed electrons impact against a substance. In color television receivers the picture tube is the main source of X-ray Radiation. This radiation can be reduced by the use of external X-ray radiation shielding and by the use of picture tubes constructed of leaded glass. If however, the receiver is operated at abnormally high voltages, excess X-ray radiation may penetrate the walls of the picture tube.

In this projection television unit the High-voltage Stabilization Circuit also performs the function of X-ray protection. For example, if Q410 is shorted and damages the High Voltage Stabilization Circuit, then High Voltage will become abnormally high as no control operation is carried out. Now it becomes necessary to detect this problem through another method in order to prevent the generation of X-rays. Therefore, the X-ray Protection Circuit used in this unit monitors the supply voltage (VCC) being applied to the high-voltage generation circuit and if it exceeds a specific value, circuit operation will be stopped. (See Fig. 3).

The output voltage (VCC) from the emitter of Q410 is divided by R473, R474, R475, R452 and is fed to the base of Q472. Additionally, the +32V reference voltage that is obtained from zener diode D420 is fed to the emitter of Q472, so that both the VCC and reference voltage are compared. At this time, the base voltage of Q472 would have been set by R452 so that Q472 remains OFF during normal operation but will turn ON if VCC exceeds a specified value.

If VCC exceeds the specified value, Q472 will turn "ON" thereby turning "ON" Q473. When Q473 is turned "ON", current flows from the emitter through R478, D473, D472 to the gate of thyristor D862 allowing D862 to turn "ON". When D862 is turned "ON", the STBY 5V flows through R874, D862, R877 and turns "ON" Q863. With Q863 turned "ON", a short exists between the base and emitter of QE05, therefore QE05 and QE06 are both turned "OFF". This de-energizes the power relay and cuts off the AC power to the main power supply of the TV set. Because thyristor D862 will remain turned "ON", the holding current continues to flow through R874/R877 and the Shut-down Mode will be maintained regardless of what else happens throughout the unit. To clear the unit from the Shut-down Mode, it's necessary disconnect the AC power cord, wait a few seconds, and re-connect the AC power.

X-RAY PROTECTION CIRCUIT

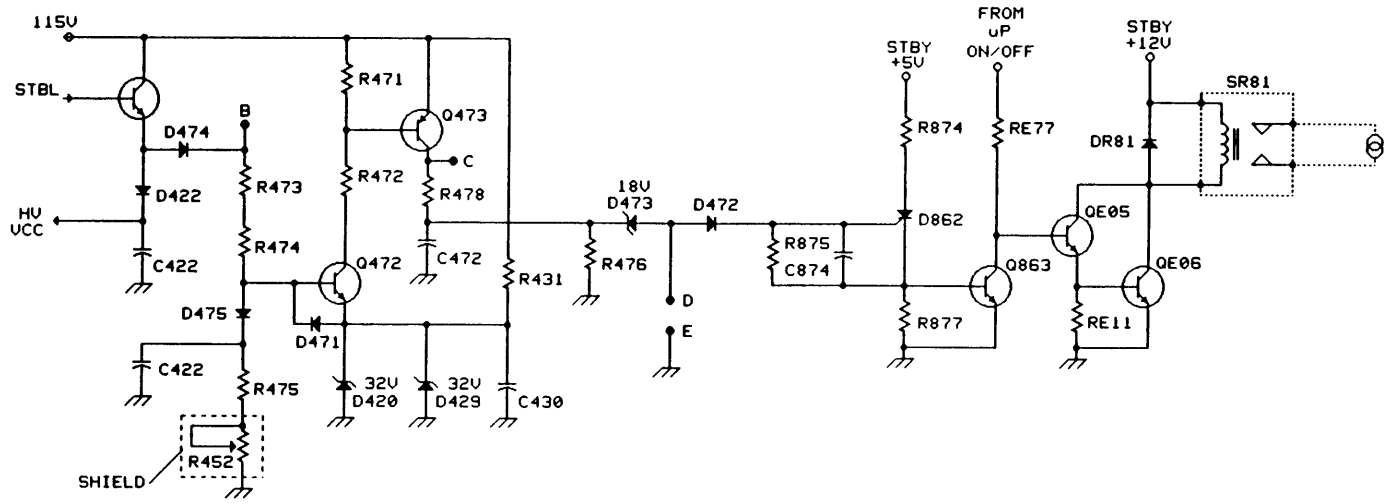


FIG. 3

X-RAY PROTECTION CIRCUIT (Cont.)

Because the emitter voltage of Q410 always has some high voltage ripple, and because spikes are developed during periods of white peak, the emitter voltage could rise above +115V. Since this is a normal operation, it is necessary to keep the protection circuit from coming ON. To keep this from happening, first the high voltage ripple is filtered by C471 at the base of Q472. Next, because Q472 and Q473 are constantly being turned ON/OFF by white peak variations of the video signal, C427 is added to the collector of Q473 and a time constant is achieved. Further, the threshold voltage of the thyristor gate (D862) is raised by Zener Diode D473 so that the thyristor can not be turned ON during the steady state.

To assure the operation of the protection circuit, R452 must be set precisely and to protect it against accidental mis-adjustment it is covered in a shielded case. R452 is adjusted by applying a specified DC voltage to test point B. This adjustment must be factory set.

Blocking diode D474 prevents any voltage applied to point B from being applied to the High Voltage Output Circuit. Blocking diode D475 prevents Q472 from being turned ON as discharge current flows to its base from C471 when the power source is turned OFF.

Because the Power Cut-off Circuit (made up of thyristor D862) puts the unit in the shut-down mode immediately, it is hard to tell whether the problem is in the Horizontal or the X-ray Protection Circuit. To isolate the problem a short must be applied between test points D and E. If the unit does not go into the shut-down mode immediately after turn-on, then the X-ray protection circuit is operating normally and the problem must be before D472.

To check the operation of the X-ray Protection Circuit, a short must be applied between test points X and R. See Fig. 4 and refer back to Fig 1. When these test points are shorted, the horizontal osc. pulse is no longer supplied to the high voltage generation circuit and no HV out is generated. This causes the detection voltage that is fed back from the FBT to the HV Stabilization Circuit to also drop. The HV Stabilization Circuit senses the drop in HV and will immediately compensate by raising the supply voltage VCC to maximum and this will force the X-ray Protection Circuit to operate.

XII.

OPTICAL SYSTEM

PROJECTION TV OPTICAL SYSTEM

Outline of Projection Tube Neck Components

Names and mounting positions of neck components of the projection tube are illustrated in Fig. 1. The neck components are (1) Deflection yoke (consisting of the main yoke, sub-yoke and centering magnet), (2) Focusing yoke, and (3) Alignment magnet.

(1). The Main Yoke of the Deflection Yoke consists of a Horizontal Deflecting Coil and a Vertical Deflecting Coil. They perform the horizontal and vertical deflection. The Sub-yoke is called a Convergence Yoke, and consist of horizontal and vertical coils. It performs distortion correction and color alignment by means of the correction current supplied from the Convergence Output Circuit. And last, the Centering Magnet. It consist of two bipolar magnets at the rear of the yoke assembly and will allow for movement of the raster position.

(2). The Focusing Yoke generates a magnetic flux that is parallel with the electron beams and focuses the beams on to the fluorescent screen. It is also equipped with a built-in coil used in performing temperature compensation and dynamic focusing.

(3). The Alignment Magnet which consists of two bipolar magnets that align the magnetic flux axis of the focus magnet to the electron beam axis from the electron gun of the projection tube. In Fig. 2, the dotted line denotes the axis of magnetic flux of the focusing yoke and the strait angle line denotes the axis of electron beam injected from the electron gun. In the case of Fig. 2, if no correction from the Alignment Magnet exists, the electron beam will be distorted because the beam does not run through the center of the Focusing Yoke/Magnet. That is why the alignment magnet corrects the beam track to get it on the Focus Magnet center axis. Therefore, the track of electron beams is corrected by bending with the alignment magnet so that it is placed on the dotted line.

PROJECTION CRT OUTLINE

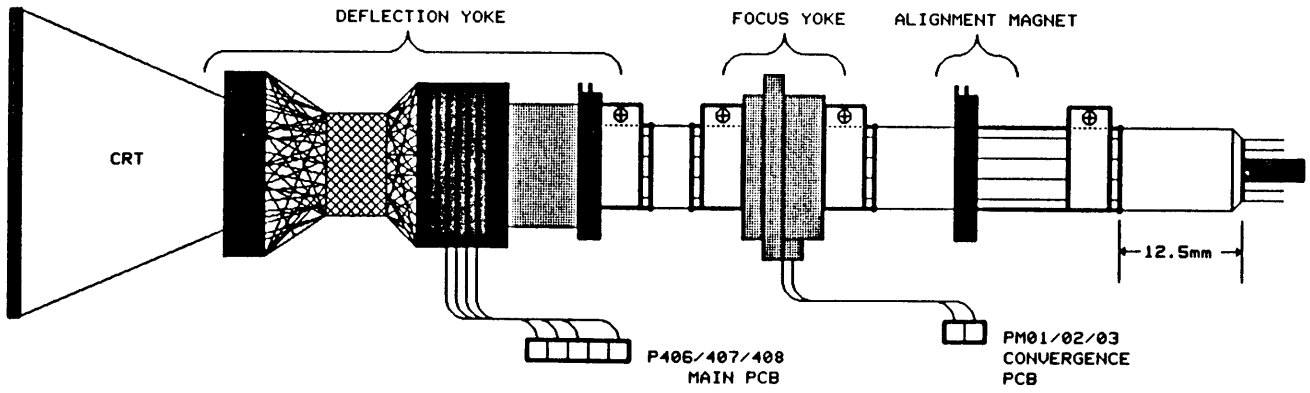


FIG. 1

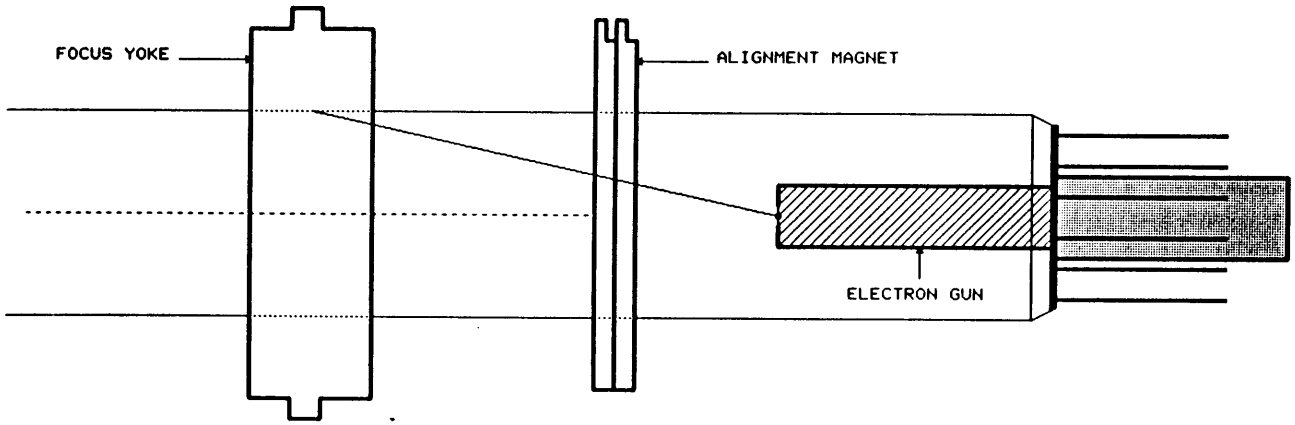


FIG. 2

PROJECTION TV OPTICAL SYSTEM (cont)

Once the track of electron beams coincides with the magnetic flux axis from the focusing yoke, actual adjustments make use of the fact that the track of electron beams does not move regardless of increase or decrease of the focusing yoke's magnetic flux.

Fig. 3A shows an example of what happens when the beam track does not coincide with the magnetic flux axis. It can be seen that the location of the beam spot moves on the CRT depending on variations in thickness of the lens (increase or decrease of the magnetic flux in the yoke). Fig. 3B, shows that when the electron beam passes through the center of the focus yoke, the location of the beam spot does not change on the CRT even though the magnetic flux is varied. To make the adjustment, a 5Hz sine wave is applied to the Focus Yoke thereby changing the magnetic flux.

FOCUS ADJUSTMENT

(1) Press the TEST/RECEIVE SW to receive the cross-hatch pattern.

(2) For easy adjustment, select the color to be adjusted on the screen. Use the lens covers to shut off the other two CRTs.

(3) Set the focus control corresponding to the color to be adjusted, to the mechanical center. (RM44 for RED, RN46 for GREEN, RM45 for BLUE). Move the focus magnet up or down on the CRT neck and fix it on the place of best focus. Repeat the adjustments of Lens-focus and Focus Magnet alternately, for best focus.

(4) Apply a 3Vp-p, 5Hz sine wave to the OSC Terminal on PW8553, and adjust the alignment magnet so that the center of the cross is positioned in the same place at the time of focusing and defocusing. Then rotate the focus control to get the best focus.

(5) Proceed with the Convergence Adjustment.

ELECTRO-MAGNETIC FOCUS

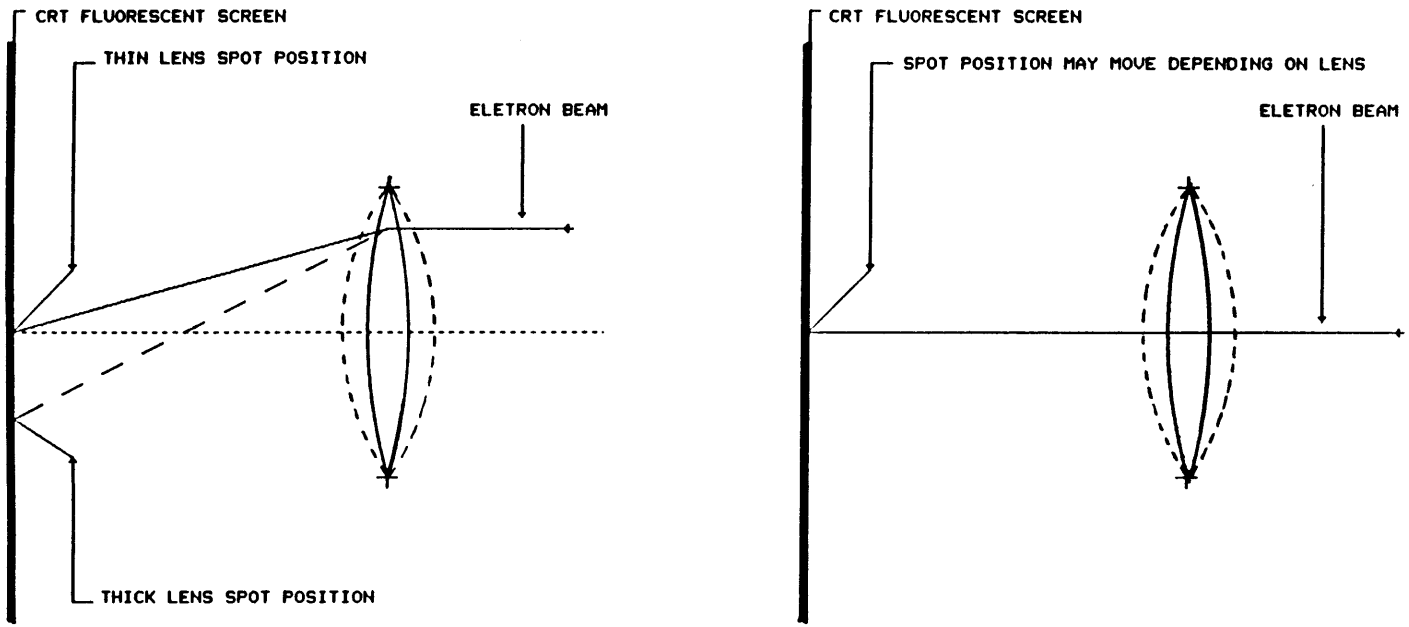
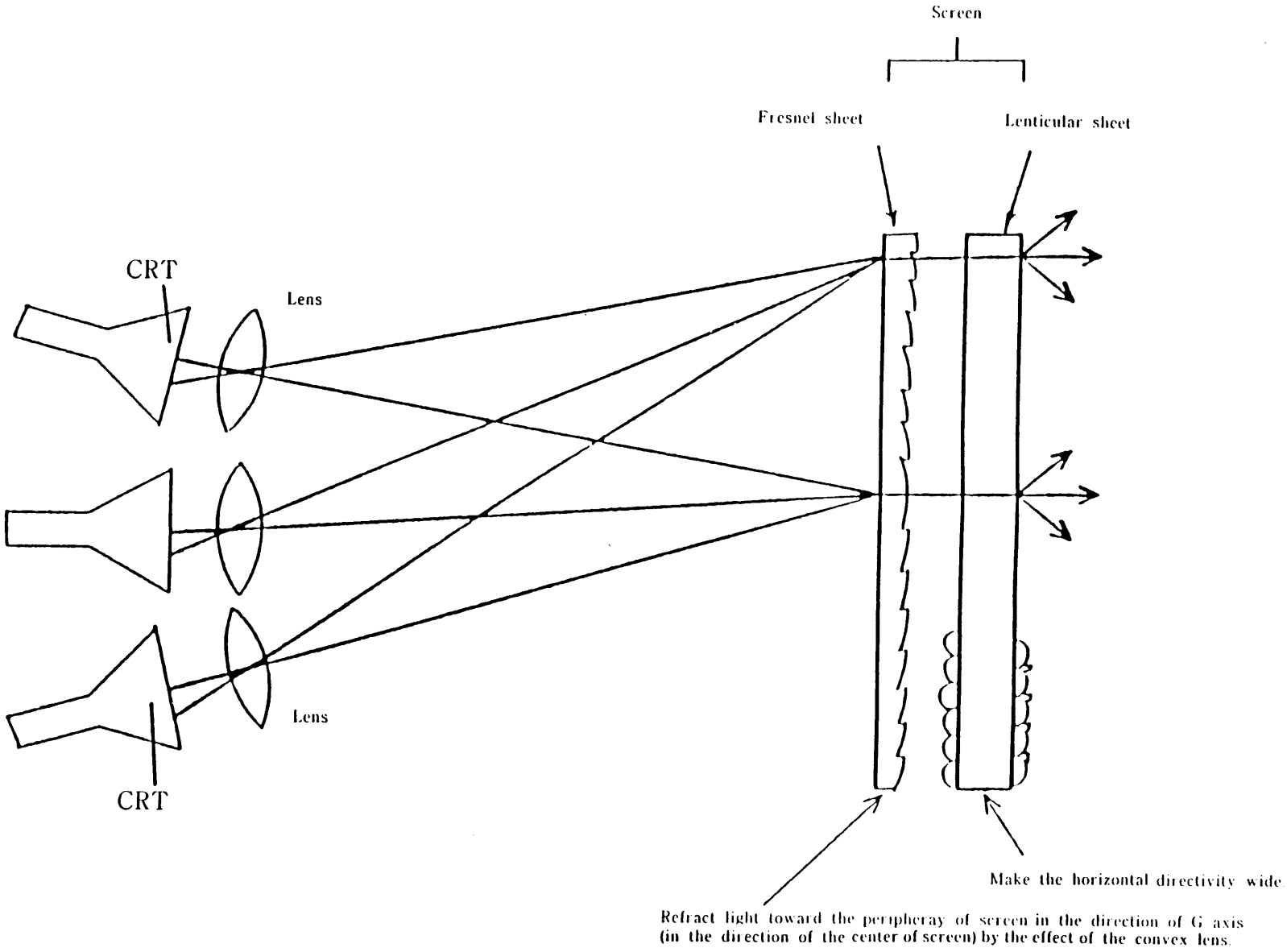


FIG. 3

FRESNEL/LENTICULAR SCREEN AFFECT



XIII.

LAB SECTIONS

HORIZONTAL DEFLECTION CIRCUIT TROUBLESHOOTING

(1) Checking the Supply Voltage (VCC); Check the +115V line from the main power source and the +33V line from the Audio Output Circuit. If no power is available, check whether the power circuit itself is out of order or the load shorted. If the horizontal output or high voltage output transistors are shorted or damaged +115V will not be supplied. If the supply voltage is normal, proceed to the following step.

(2) Checking the Horizontal Start-up Circuit; Check for the +8V at the cathode side D340. If missing, check Q400 and its peripheral parts, Q501 pin 9, D401, C410, etc. If they check OK, proceed to the next step.

(3) Checking the Horizontal Oscillator Circuit; Check and see if a square wave signal at the horizontal rate outputs pin 10 of Q501. If missing replace Q501. If the signal is available, proceed to the next step.

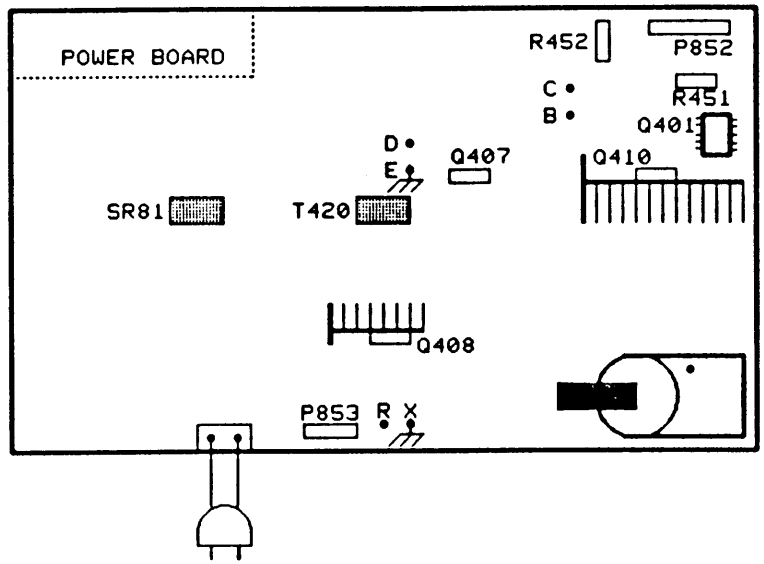
(4) Checking the Horizontal Drive Circuit; Check and see if the oscillator signal is at the base and collector of the horizontal drive transistor (Q402). If present, confirm that the signal inputs and outputs the driver transformer (T401). If the signal is missing at the secondary, T401 may be defective or a short-circuit between the base and emitter of the output transistor may exist. If the output circuit does not operate even though the oscillator signal is present at the base of Q404 then the horizontal output transistor may be defective (open base to emitter).

(5) Trouble in the Pulse Transformer's output power circuits; When the symptom "No Raster" appears, there is the possibility that the problem could be caused by trouble in one of the power lines tapped from the Horizontal Output Transformer (T462). So in addition to checking the Main Power Circuit it is also necessary to check all the power lines supported by the Horizontal Output Circuit. All of the power lines coming out of T462 are connected to protective resistors.

FS CIRCUIT CHECK

The Fail Safe (FS) Circuit check is an important part of the final check after servicing. The circuit should be checked following the steps below. For test point location see figure below.

(1) Turn the receiver ON.
(2) On the Power Board temporarily short TP-R (Hor. Osc. Signal to the base of the H.V. Drive Tx) to TP-X (Gnd). Raster and sound will disappear.
(3) The receiver must remain in this state even after removing the short from the test points. This is evidence that the FS Circuit is functioning properly.
(4) To obtain normal operation again, temporarily disconnect the AC power to the receiver and allow the FS Circuit over 5 seconds to reset. Then reconnect the AC power and the set should turn on.



HIGH VOLTAGE CIRCUIT
TROUBLESHOOTING PROCEDURES

Problems when the X-ray Protection Circuit operates are described below.

A. When the High-voltage Control Circuit becomes defective:
   1. Check for short circuit between the collector and the emitter of Q409 and Q410.
   2. Check for short circuit between the base and the emitter of Q405 or open collector or open R445.
   3. Check for open or damaged D421.
   4. Check for damaged Q401.
   5. Check for short or damaged D420 and D429.

B. When the High-voltage Generation Circuit is defective
   1. Check for damage to buffer transistors Q420/Q415 and/or connections between the Horizontal Oscillator Circuit and the High-voltage Generating Circuit.
   2. Check for damage to the high-power drive transistor Q407.
   3. Check for short circuit or open between the base and emitter of the high-voltage output transistor Q408 or open in the collector circuit.
   4. Check for damaged FBT.

C. When the X-ray Protective Circuit is defective:
   1. Check for short circuit between the collector and emitter of Q472.
   2. Check for short circuit between the collector and emitter of Q473.
   3. Check for short or damaged D473.

D. Other circuits than will affect the High-voltage Circuit are:
   1. When the Horizontal Start-up Circuit is damaged. A pulse is no longer supplied to the High-voltage Generating Circuit and the same operation as when R and X terminals are shorted is performed.

HIGH VOLTAGE CIRCUIT TROUBLESHOOTING (Cont.)

2. When +12V power is unavailable. Supply voltage is no longer supplied to Q415 and IC Q401 and the same state as in (1) results.
3. When +9V power is unavailable. As Q420 is disabled and the same state as in (1) results.
4. When the Horizontal Pulse or +12V power is no longer supplied to the Power Supply PCB because of an open in the wiring harness.

In case of the following troubles, replace the Power PCB with a factory adjusted unit.

(1) When the FBT is defective:
The FBT houses a resistor to detect high-voltage, its resistance value varies. Normal high voltage is not obtained by simply replacing the FBT, it is necessary to readjust R451 using a high-voltage meter.

(2) When IC Q401 (TA75559P) is defective:
High-voltage may change due to offset voltage fluctuation of the operational amplifier.

(3) When D420 and D429 are defective:
The reference voltage may change, resulting in changes in the high voltage. In addition, the operating point of the X-ray protection circuit may also change.

(4) When D421 and Q455 are defective:
High-voltage may change due to fluctuation in zener voltage and base-to-emitter voltage.

(5) If any one of these: R426, R432, R433, R451, R473, R474, R475 and R452 are replaced, the high-voltage and the operating point of the X-ray protective circuit may change.

VERTICAL DEFLECTION CIRCUIT TROUBLESHOOTING

Because of the protection circuit built in the Vertical Deflection, it is possible that the symptom of "No Picture (Raster)" can be traced back to a Vertical Deflection problem.

As an initial check, if the Horizontal Deflection Circuit and the High Voltage Circuit are operating, check the collector voltage of Q342 and if it reads about 12VDC then it is possible that the Vertical Deflection Circuit is inoperative. Follow the steps listed below:

(1). Check the deflection coils and see if any of the connectors are loose or an open deflection coil (vertical deflection coils are mounted in series). If OK, proceed to the next check.

(2). Check the supply voltage to the Vertical Output Circuit. The voltage at pin 7 of Q301 should read 27V. If not, check R327. If OK, proceed to the next check.

(3). Check the Vertical Output Circuit operation. Observe the waveform at pin 2 of Q301 (TP-82). If the waveform is incorrect or missing, check the input signal waveform at pin 4 of Q301. The input signal should also be checked at pin 35 of Q501. If there is an input signal but no output signal, then replace Q301. If there is no input signal, proceed to the next check.

(4). Check the 9V power supply. Pin 27 of Q501 should read 9VDC. If not. check the 9V power circuit.

(5). Check the Sawtooth Voltage Generating Circuit. A sawtooth waveform should be available at pin 36 of Q501. If waveform is incorrect or missing, check the voltage at pin 1 of Q501. It should read about 1.4 VDC. If the voltage is missing, replace Q501. If the voltage is OK at pin 1, then go on and check the voltage at pin 2 of Q501. It should read about 4.3VDC. If this voltage is missing, check the feedback circuit and/or replace Q301.

POWER SUPPLY CIRCUIT TROUBLESHOOTING

A. Measurement Precautions

THE PRIMARY SIDE OF THE SWITCHING POWER SUPPLY IS NOT ISOLATED FROM THE A.C. LINE NECESSITATING THE USE OF AN ISOLATION TRANSFORMER.

To prevent erroneous measurements, care must be taken as to where test equipment is grounded.

a. For measurement of points on the Primary side, a ground common to the primary side must be used.
b. For measurement of points on the secondary side, a ground common to secondary side must be used.

B. System Shutdown (No Secondary Supplies)

a. Check Fuses
b. Check Bridge Rectifier Output
c. Check Start up Resistor
d. Check Continuity of the transformer
e. One shorted secondary supply may cause shutdown of the regulator I.C.. Disconnect Secondary supplies at the transformer one at a time while monitoring other supplies to see if they begin operation. Troubleshooting defective secondary supply.

USE ON A VARIAC MAY BE HELPFUL, DEFECTIVE COMPONENT MAY NOT DRAW ENOUGH CURRENT AT LOW VOLTAGE TO CAUSE SHUTDOWN.

C. Secondary Supply Shutdown

a. Disconnect the load from the supply load to determine if malfunction is in the load or the supply. Troubleshooting defective circuit.

D. Ripple In the Supply

a. Check Bridge Rectifier and Filter Capacitors
b. Check Feedback circuit, Stabilizer circuit, especially Detector Rectifier. This also may cause fluctuation in the secondary supplies.

NO CARVER EXPANSION EFFECT IS HEARD (POSSIBLE NUISANCE CALL)

IS THE AUDIO SIGNAL INPUT IN STEREO? — NO → THE CARVER SYSTEM WILL BE AFFECTED BY ITS SOURCE. LISTEN TO A STEREO SOURCE.

YES ↓

ANY DIFFERENCE HEARD WHEN THE CARVER SW IS TURNED ON/OFF?

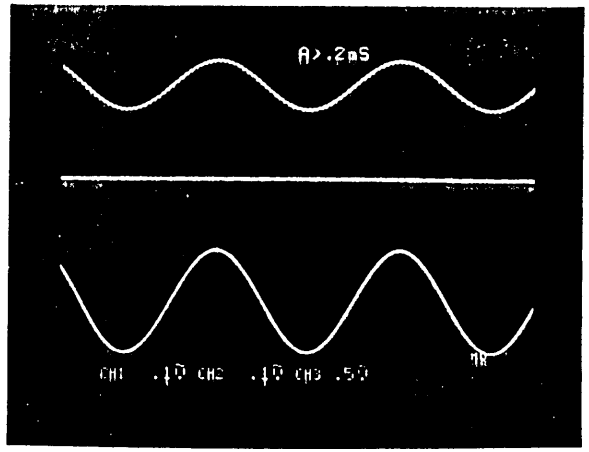
NO ↓

CHECK THE CONTROL SIGNAL FROM THE uP AT PIN 4 OF PC02
CARVER ON → H = 3V CARVER OFF → L = 0V — NO → CHECK THE uP ICA01

YES ↓

1. CONNECT A SINE WAVE OF 400Hz, 400mV RMS TO THE E1 INPUT R Ch MONITOR THIS INPUT ON CH3 OF SCOPE. TRIGGER ON Ch 3
2. CONNECT Ch 1 OF SCOPE TO CARVER PC R Ch OUT. PC02 #5
3. CONNECT Ch 2 OF SCOPE TO CARVER PC L Ch OUT. PC02 #6
4. TURN SET ON (CARVER OFF) AND OBSERVE WAVEFORMS
5. TURN CARVER ON, OBSERVE WAVEFORMS AND MAKE COMPARISON HOW MUCH PHASE SHIFT IS THERE BETWEEN Ch1, Ch2, & Ch3.

CARVER OFF

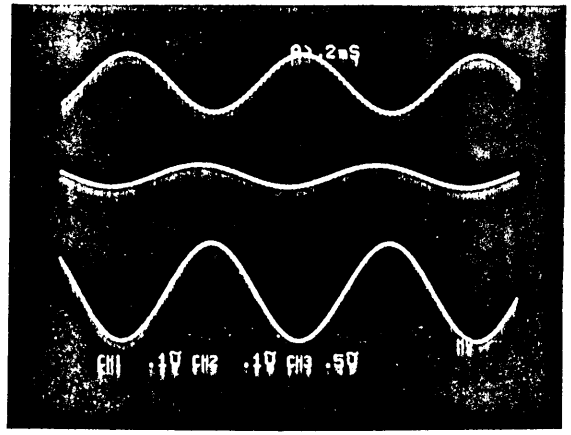


CH 1 R Ch OUT

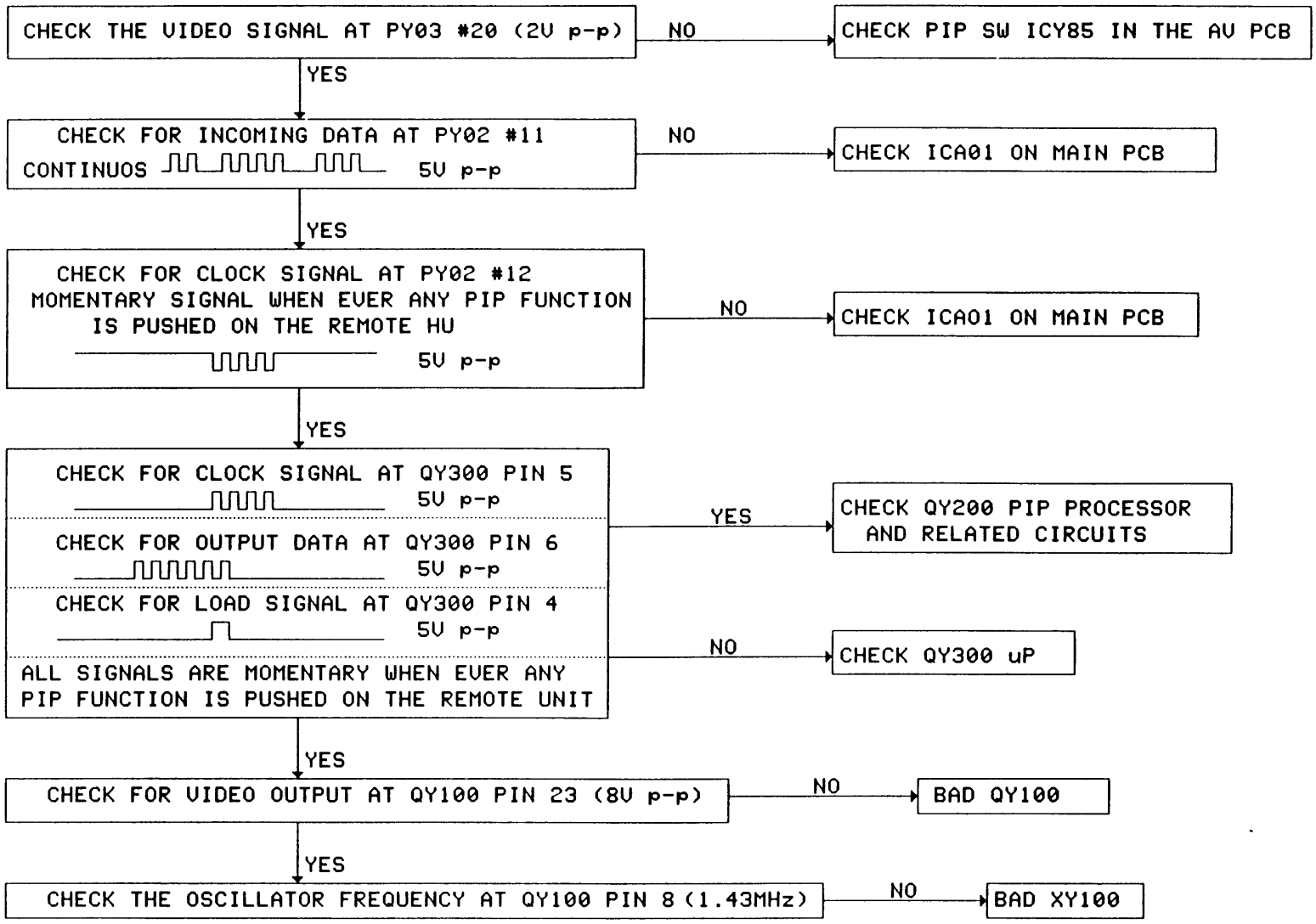
CH 2 L Ch OUT

CH 3 R Ch IN

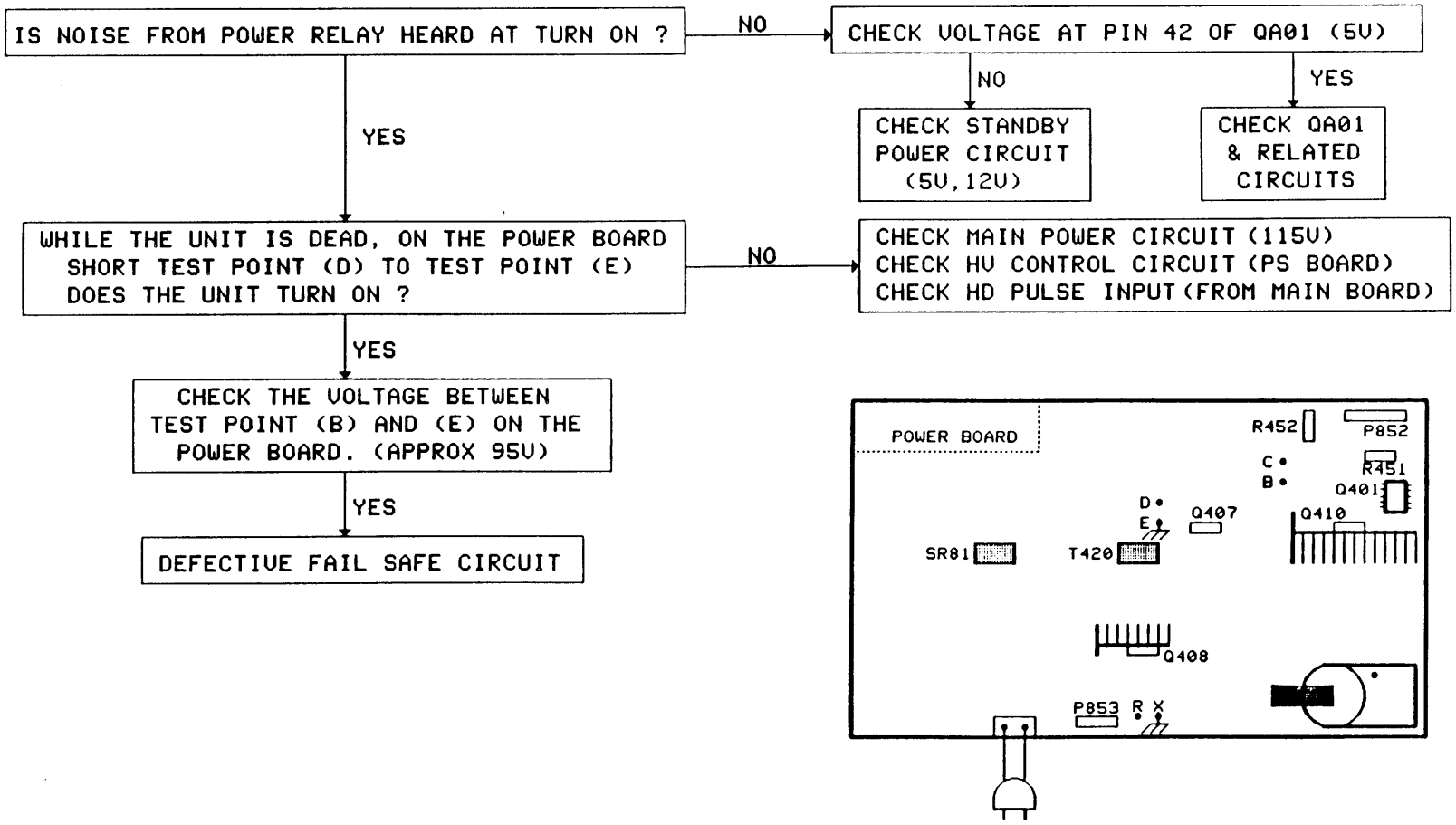
CARVER ON



NO OR BAD PIP


CHECK THE VIDEO SIGNAL AT PY03 #20 (2V p-p)
NO
CHECK PIP SW ICY85 IN THE AV PCB
YES
CHECK FOR INCOMING DATA AT PY02 #11
CONTINUOS
5V p-p
NO
CHECK ICA01 ON MAIN PCB
YES
CHECK FOR CLOCK SIGNAL AT PY02 #12
MOMENTARY SIGNAL WHEN EVER ANY PIP FUNCTION
IS PUSHED ON THE REMOTE HU
5V p-p
NO
CHECK ICA01 ON MAIN PCB
YES
CHECK FOR CLOCK SIGNAL AT QY300 PIN 5
5V p-p
CHECK FOR OUTPUT DATA AT QY300 PIN 6
5V p-p
CHECK FOR LOAD SIGNAL AT QY300 PIN 4
5V p-p
ALL SIGNALS ARE MOMENTARY WHEN EVER ANY
PIP FUNCTION IS PUSHED ON THE REMOTE UNIT
YES
CHECK QY200 PIP PROCESSOR
AND RELATED CIRCUITS
NO
CHECK QY300 uP
YES
CHECK FOR VIDEO OUTPUT AT QY100 PIN 23 (8V p-p)
NO
BAD QY100
YES
CHECK THE OSCILLATOR FREQUENCY AT QY100 PIN 8 (1.43MHz)
NO
BAD XY100

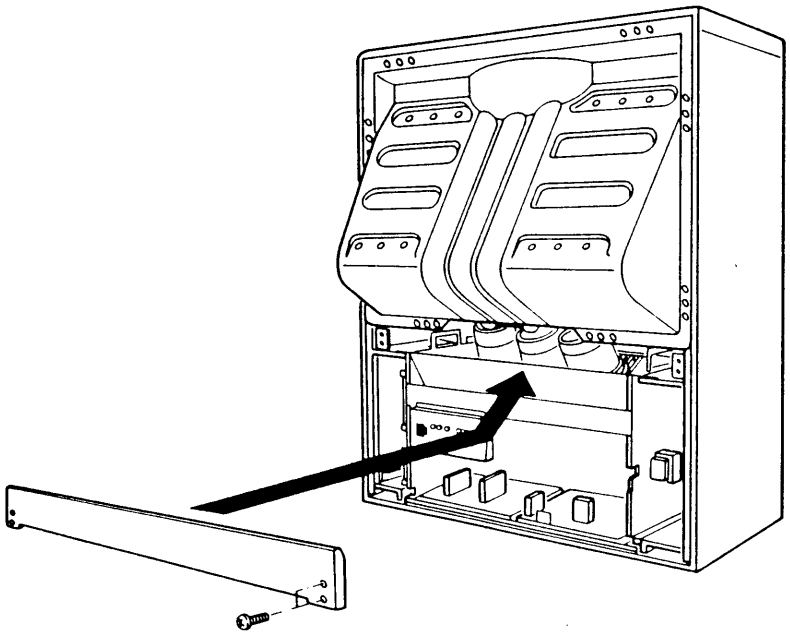
UNIT DEAD

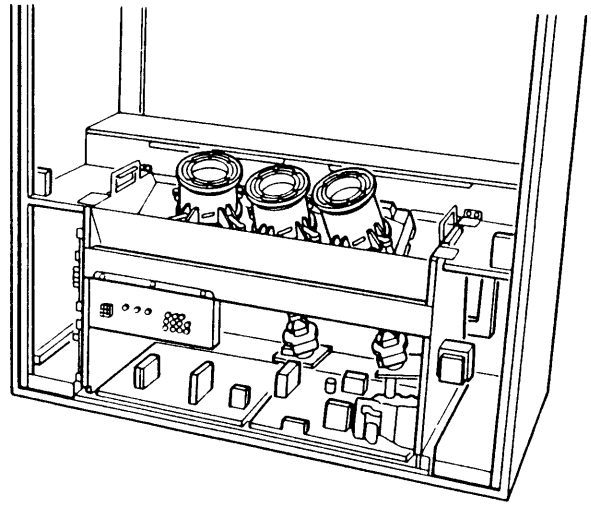

IS NOISE FROM POWER RELAY HEARD AT TURN ON ?
NO
CHECK VOLTAGE AT PIN 42 OF QA01 (5V)
NO
YES
CHECK STANDBY POWER CIRCUIT (5V, 12V)
CHECK QA01 & RELATED CIRCUITS
YES
WHILE THE UNIT IS DEAD, ON THE POWER BOARD SHORT TEST POINT (D) TO TEST POINT (E) DOES THE UNIT TURN ON ?
NO
CHECK MAIN POWER CIRCUIT (115V)
CHECK HV CONTROL CIRCUIT (PS BOARD)
CHECK HD PULSE INPUT (FROM MAIN BOARD)
YES
CHECK THE VOLTAGE BETWEEN TEST POINT (B) AND (E) ON THE POWER BOARD. (APPROX 95V)
YES
DEFECTIVE FAIL SAFE CIRCUIT
POWER BOARD
R452
P852
C
B
R451
Q401
D
E
Q407
Q410
SR81
T420
Q408
P853
R
X

SCREEN AND LIGHT BOX REMOVAL

ON THE 52 INCH SET THE SCREEN MOUNTING SCREWS ARE EASILY VISIBLE FROM THE FRONT
ON THE 46 INCH SET HOWEVER THE FRONT MOULDING ON TOP OF THE SCREEN MUST BE REMOVED
TO EXPOSE THE MOUNTING SCREWS. VERY CAREFULLY PRY THE TOP MOULDING UPWARDS EVENLY
AT BOTH ENDS AND LIFT UP.

1. TO REMOVE THE LIGHT BOX, START BY REMOVING THE BACK BOARD AND THE BACK SUPPORT FRAME.
2. REMOVE FRONT GRILLE AND CONVERGENCE ASSEMBLY. AND CLEAR THE WIRES FRON THE WIRE HARNES
3. REMOVE MOUNTING SCREWS. THREE ON BOTTON AND FOUR ON FRONT
4. DISCONNECT P690 (SPEAKER PLUG) AT THE A/V BOARD AND CLEAR THE WIRES FRON THE WIRE HARNES
5. REMOVE THE REMOTE SENSOR AND FRONT CONTROL BOARDS FROM THE FRONT DOOR ASSEMBLY AND CLEAR THE WIRES FROM THE WIRE HARNES
6. PULL LIGHT BOX BACK AND OUT





CRT REMOVAL AND SET UP

1. REMOVE MIRROR BACK

2. REMOVE FRONT SPEAKER GRILL AND CONVERGENCE PCB

3. FROM THE FRONT, REMOVE THE CRT DRIVE PCB AND GND

4. REMOVE CRT 2nd ANODE LEAD. BE VERY CAREFULL WHEN CUTTING AWAY THE RTV AS NOT TO DAMAGE THE ANODE PLUG

5. DISCONNECT THE YOKE PLUG FROM THE MAIN PCB AND CLEAR IT FROM THE WIRE HARNESS

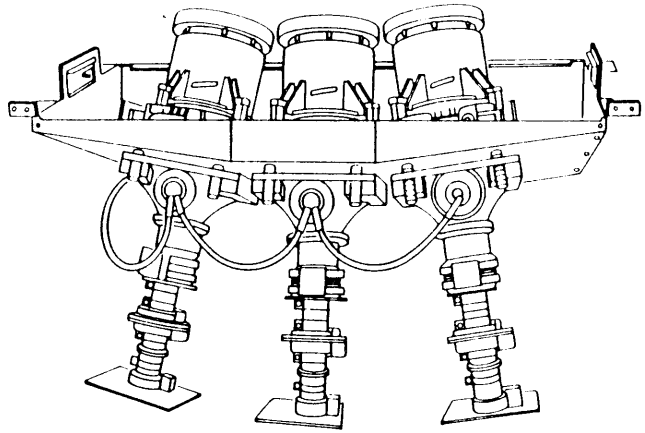
6. DISCONNECT THE CONVERGENCE AND FOCUS MAGNET PLUGS FROM THE CONVERGENCE PCB AND CLEAR THEM FROM THE WIRE HARNESS

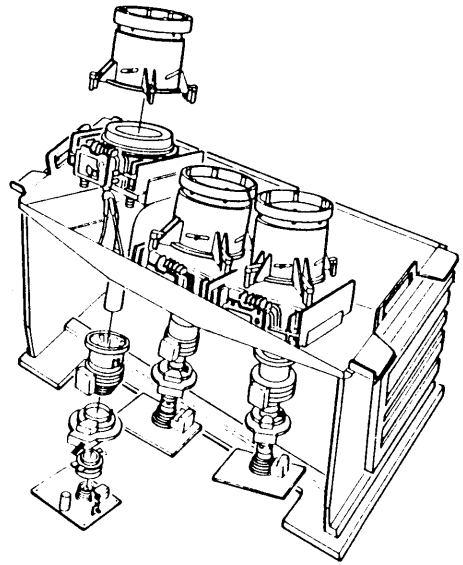
7. FROM THE BACK, REMOVE THE FOUR CRT MOUNTING SCREWS

8. REMOVE CRT

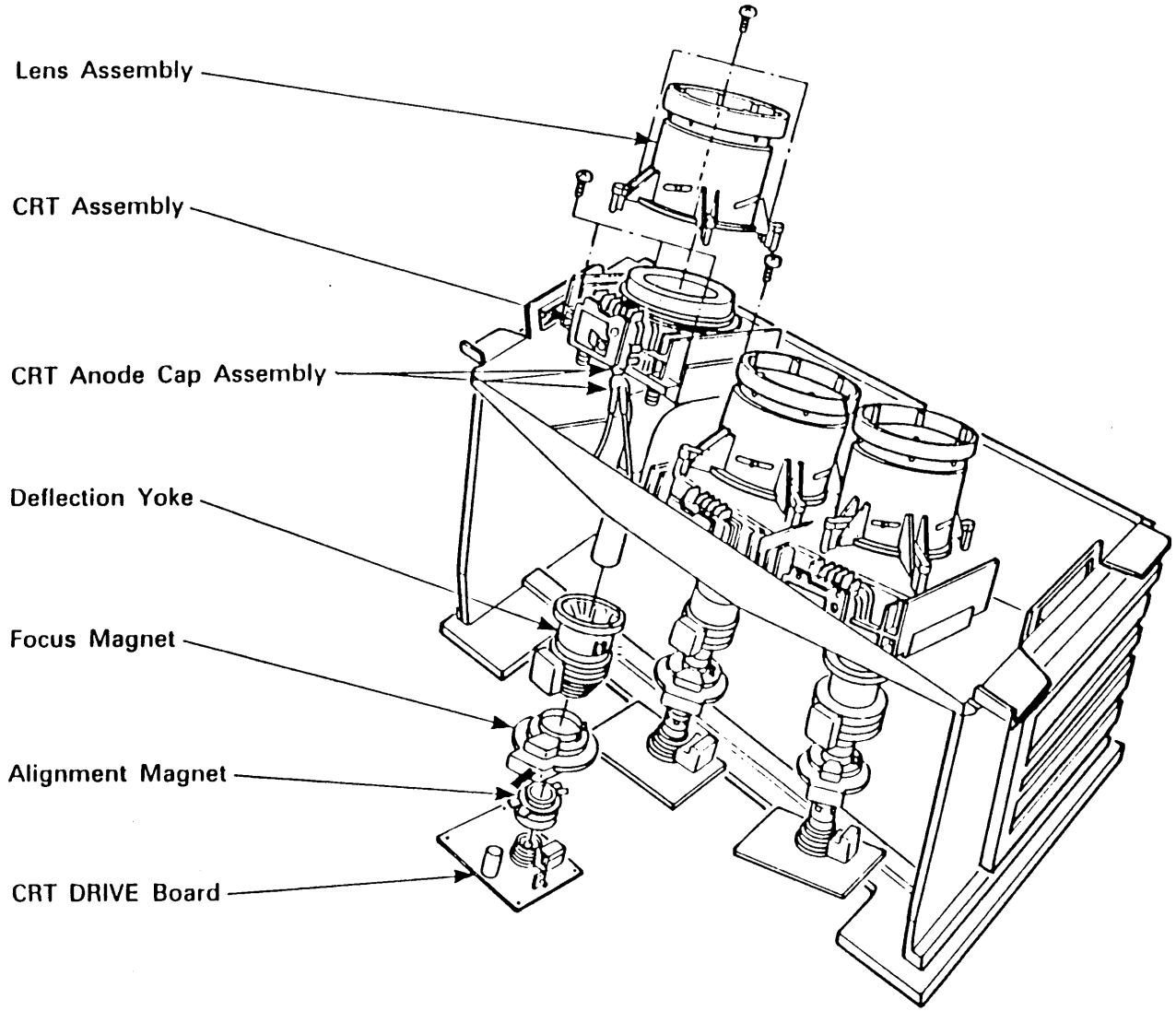
9. TRANSFER LENS, YOKE, AND MAGNET ASSEMBLIES TO NEW CRT AS CLOSE AS POSIBBLE TO THE POSITIONING IN THE OLD CRT AND FOLLOW THE ABOVE PROCEDURE IN REVERSE
   NOTE; WHEN RECONNECTING THE SECOND ANODE LEAD IT MUST BE SEALED WITH A HIGH VOLTAGE RTV COMPOUND PN 23192770

10. CONTINUE WITH THE SET-UP PROCEEDURE LISTED
    A) PICTURE TUBE COMPONENTS ADJUSTMENT
    B) ELECTRIC FOCUS ADJUSTMENT
    C) CONVERGENCE ADJUSTMENT
    D) GRAY SCALE AJUSTMENT





LIGHT BOX COMPONENTS



PICTURE TUBE COMPONENTS ADJUSTMENT SEQUENCE

(1) Lens Focus coarse adjustment
(2) Focus Coil coarse adjustment
(3) Centering Magnet coarse adjustment
(4) Alignment Magnet fine adjustment
(5) Deflection Yoke Inclination fine adjustment
For G, P704 is connected. For R, P702 is connected. For B, P703 is connected.
(6) Distortion adjustment (G only)
(7) Vertical Height adjustment (G only)
(8) Horizontal Width adjustment (G only)
(9) Vertical Lin. adjustment (G only)
(10) Centering Magnet fine adjustment (Repeat procedures 6 to 10)
(11) Lens Focus fine adjustment (center of screen)
(12) Focus Control fine adjustment
(13) Centering Magnet fine adjustment

Note:
* When adjusting the yoke inclination, disconnect P702 for R Dynamic Convergence, and P703 for B Dynamic Convergence.
* When adjusting the centering magnet, connect the dynamic convergence.
* Static convergence is always off until the Dynamic Convergence Adjustment is completed (PJ03).
* If the picture position can not be set to the center of the screen by adjusting the centering magnet, move the focus coil to readjust the alignment magnet.

CONVERGENCE

To be performed anytime the CRTs, yokes, or focus coils are moved or replaced. Assume that the green CRT has been changed.

1. Press the customer control test pattern button, a cross pattern will appear. See Fig. 1.

2. Cover red and blue CRTs (green CRT set-up).

3. Connect an OSC to the convergence board (5 to 10Hz 3Vp-p signal) to TP-OSC terminal and TP-GND. See Fig. 2. The cross pattern will now move on the screen. A good source for this is an audio signal generator.

4. Adjust the alignment magnet on the neck of the CRT near the socket (see Fig. 3) so that the pattern moves at its slowest rate.

5. Disconnect the oscillator (pattern will stop moving).

6. Adjust the focus coil (use a non-magnetic driver on the clamps screws). By moving the coil back and forth you can adjust for best focus. By rotating the coil clockwise, you can adjust the centering. Once the pattern has been centered and focused, the clamp can be tightened.

7. On the convergence board adjust the green focus pot (RM46) for best focus.

8. If necessary adjust the focus lens on the CRT face by loosening the wing nut and rotating the focus lens back and forth for best focus. (2 persons or a mirror are necessary)

9. Again, readjust the focus pot in the convergence board.

10. Adjust yoke for proper tilt. Loosen the yoke clamp. Push yoke all the way up on the CRT neck, and rotate it so that the pattern is at its most horizontal point (tighten clamp).

11. Now proceed with the convergence on the green CRT.

FIG. 1

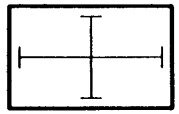
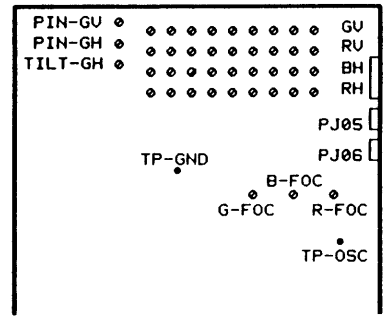


FIG. 2



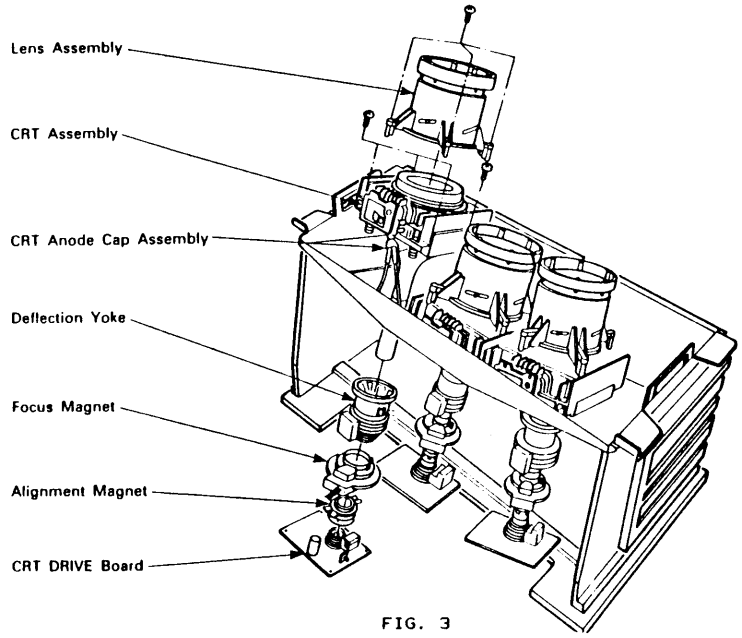


FIG. 3

12. The pincushion and tilt adjustments are necessary on the green CRT only, as adjustment is for all three CRTs.
    a) On the convergence board disconnect PJ05 (white) and connect it to PJ06 (black). A cross hatch pattern will appear on the screen. Now the three pots: TILT-GH, PIN-GH, PIN-GV can be adjusted.
    b) Adjust PIN-GH. The sides of the pattern will move in and out, adjust it so that the left and right side lines are straight up and down. See Fig. 4
    c) Adjust PIN-GV, the top and bottom of the pattern will move in and out, adjust it so that the top and bottom lines are at their most horizontal point. See Fig. 5
    d) Adjust TILT-GH, the whole pattern will tilt from side to side. Adjust it so that the picture is at its most square point. See Fig 6.

Now the blue can be converged onto the green.

13. Disconnect the plug from PJ06; and reconnect it to PJ05 (cross pattern will reappear on the screen). Remove cover from blue CRT.

14. Disconnect P703 on the convergence board. (This will disconnect the front panel controls) Because it is the green CRT that has been changed, it will be converged on to the blue.

15. Adjust the green centering magnet on the green CRT so that the green cross is converged on top of the blue concentrating on the center of the screen.

16. Disconnect the plug from PJ05 and connect it to PJ06, also reconnect plug P703 and disconnect PJ03.

Now proceed to converge the blue onto the green using the BH controls.

17. Adjust RK40 (TILT) and RK44 (BOW) concentrating on the "center vertical line" and converge the blue line onto the green. See Fig. 7.

18. RK48 (KEY) controls the outer most line on the right hand side. Adjust RK48 so that the blue line is at its most parallel point to the green and not necessarily converged on top of it. See Fig. 8.

19. RK52 (S KEY) controls the outer most line on the left hand side. Adjust RK52 so that the blue line is at its most parallel point to the green and not necessarily converged on top of it. See Fig. 9.

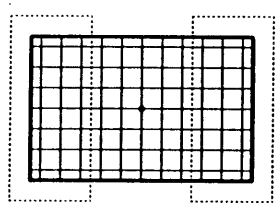


FIG. 4

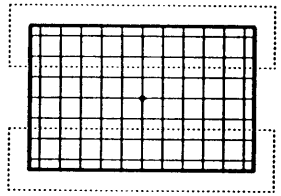


FIG. 5

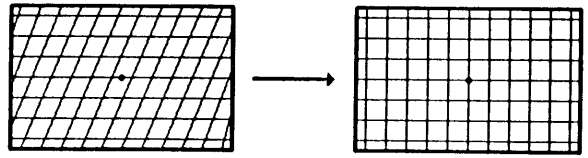


FIG. 6

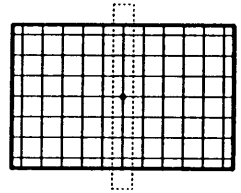


FIG. 7

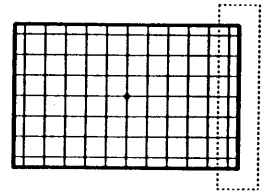


FIG. 8

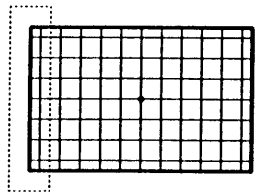


FIG. 9

20. RK56 (PIN) controls the outer most line on the right hand side. Adjust RK56 to eliminate any bowing and make the blue line as parallel as possible to the green. See Fig. 10.

21. RK60 (S PIN) controls the outer most line on the left hand side. Adjust RK56 to eliminate any bowing and make the blue line as parallel as possible to the green. See Fig. 11.

22. RK64 (LIN) controls the blue line at both the right and left hand side. Adjust RK64 so that the blue is on the opposite sides and at the same distance away from the green. (So the blue can be on either the inside or outside of the blue on both sides but the distance must be the same to both sides from the green.) See Fig. 12.

23. RK68 (SIZE) controls the blue line at both sides of the screen. Adjust RK68 so that the blue line at both the right and left hand sides become converged on top of the green. You may have to go back and forth between RK64 and RK68 to get the best convergence on left and right.

24. RK72 controls the areas half way to the center and the sides. Adjust RK72 for optimum condition is these areas. See Fig. 13.

25. Check the overall convergence and go back to each pot that might need retouching.

Now proceed with the blue vertical convergence using the BV controls. If at any point the center goes out of convergence, go back to the centering magnet on the CRT and readjust it.

26. Adjust RJ67 (TILT) and RJ71 (BOW) concentrating on the center horizontal line and converge the blue line on to the green. See Fig. 14.

27. RJ75 (KEY) controls the blue line along the bottom of the screen. Adjust RJ75 so that the bottom line at the right and left hand sides become equal distance and on the same side of the green. See Fig. 15.

28. RJ79 (S KEY) controls the blue line along the top of the screen. Adjust RJ79 so that the top line at the right and left hand sides become equal distance and on the same side of the green. See Fig 16.

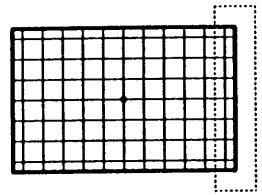


FIG. 10

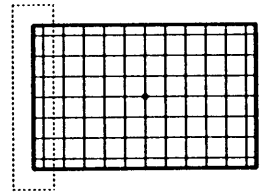


FIG. 11

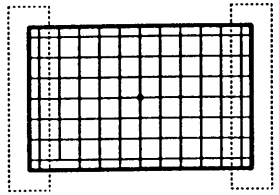


FIG. 12

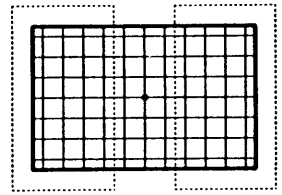


FIG. 13

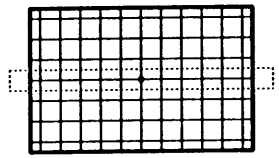


FIG. 14

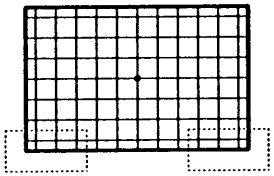


FIG. 15

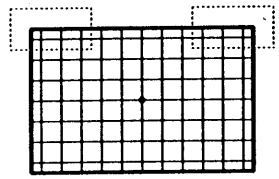


FIG. 16

29. RJ83 (PIN) controls bowing of the blue line along the bottom of the screen. Adjust RJ83 so that the blue line is at the bottom of the screen at its most parallel point to the green and not necessarily converged on top of it. See Fig. 17.

30. RJ114 (S PIN) controls bowing of the blue line along the top of the screen. Adjust RJ114 so that the blue line along the top of the screen is at its most parallel point to the green and not necessarily converged on top of it. If the tilt on the left or right hand side are not correct, go back and retouch the pots controlling these areas. See Fig 18.

31. RJ87 (LIN) controls the blue line at the top and bottom. Adjust RJ87 so that the blue line is on the opposite side and at the same distance away from the green. (So the blue line can be either on the inside or outside of the green line but the distance must be the same at both sides.) See Fig. 19.

32. RJ91 (SIZE) controls the blue line at both top and bottom of the screen. Adjust RJ91 so that both the top and bottom blue lines become converged on top of the green. You may have to go back and forth between RJ87 and RJ91 to get the best convergence on top and bottom.

33. RJ118 (C KEY) controls the four corners. Adjust RJ118 for optimum convergence at the corners of the screen. See Fig. 20.

34. Recheck the overall convergence of the screen and go back and retouch any of the controls as needed.

35. Reconnect PJ03 for front panel control operation. Remove all CRT shields and adjust the front panel controls so that the blue, red, and green are all converged.

36. Disconnect plug from PJ06 and reconnect it to plug PJ05 (cross pattern will appear). See Fig. 21.

37. Proceed with Gray Scale adjustment.

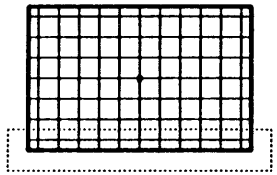


FIG. 17

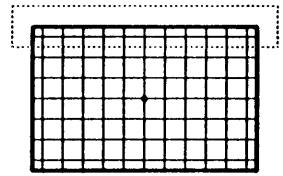


FIG. 18

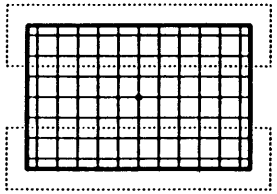


FIG. 19

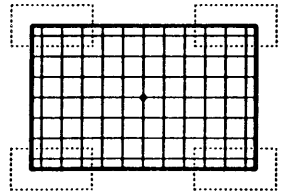


FIG. 20

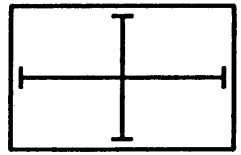


FIG. 21

CRT GRAY SCALE ADJUSTMENT

(1) Tune in an active channel.

(2) Set the COLOR Control to minimum.

(3) Turn the BRIGHTNESS & CONTRAST controls to minimum.

(4) Set the SERVICE SW on the G-DRIVE Board to the "SERV." position. The picture will become a raster only. (Colors R/B remain.)

(5) Put the covers on the R&B lens.

(6) Gradually rotate the G-SCREEN control clockwise until the raster appears slightly on the screen.

(7) Set the SERVICE SW to the "NORM" position. (A normal green picture will appear.)

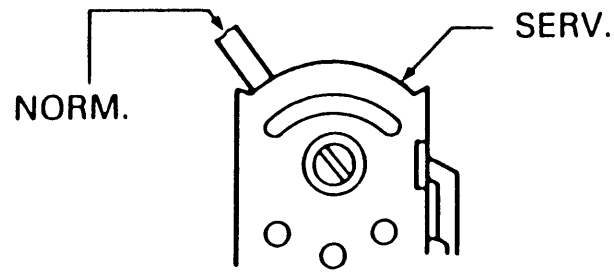
(8) Remove the covers on the R&B lens.

(9) Adjust the R-SCREEN (R953) & the B-SCREEN (R955) controls until a dark gray raster is achieved.

(10) Set the TV to "RESET" using the remote hand unit.

(11) Adjust the R-DRIVE (R950) & B-DRIVE (R952) controls (on the CRT drive PCB's) for a proper white-balance picture in the high lite area.

(12) Check the white balance in both low and high light areas. If necessary, perform steps 9 to 11.



LAB TROUBLESHOOTING UNIT #____

Audio Normal? Yes __ No __ Video Normal? Yes __ No __
Color Normal? Yes __ No __ Raster Normal? Yes __ No __

Symptoms:

_____

_____

_____

Suspected Circuit area:

_____

_____

Tests and Measurements

Mode	Test point	Signal	Mode	Test point	Signal

Diagnosis:

_____

_____

Corrective action:

_____

_____

LAB TROUBLESHOOTING UNIT #____

Audio Normal? Yes ___ No ___ Video Normal? Yes ___ No ___
Color Normal? Yes ___ No ___ Raster Normal? Yes ___ No ___

Symptoms:

_____

_____

_____

Suspected Circuit area:

_____

_____

Tests and Measurements

Mode	Test point	Signal	Mode	Test point	Signal

Diagnosis:

_____

_____

Corrective action:

_____

_____

LAB TROUBLESHOOTING UNIT #____

Audio Normal? Yes __ No __ Video Normal? Yes __ No __
Color Normal? Yes __ No __ Raster Normal? Yes __ No __

Symptoms:

_____

_____

_____

Suspected Circuit area:

_____

_____

Tests and Measurements

Mode	Test point	Signal	Mode	Test point	Signal

Diagnosis:

_____

_____

Corrective action:

_____

_____

LAB TROUBLESHOOTING UNIT #_____

Audio Normal? Yes ___ No ___ Video Normal? Yes ___ No ___
Color Normal? Yes ___ No ___ Raster Normal? Yes ___ No ___

Symptoms:

_____

_____

_____

Suspected Circuit area:

_____

_____

Tests and Measurements

Mode	Test point	Signal	Mode	Test point	Signal

Diagnosis:

_____

_____

Corrective action:

_____

_____

LAB TROUBLESHOOTING UNIT #____

Audio Normal? Yes __ No __ Video Normal? Yes __ No __
Color Normal? Yes __ No __ Raster Normal? Yes __ No __

Symptoms:

_____

_____

_____

Suspected Circuit area:

_____

_____

Tests and Measurements

Mode	Test point	Signal	Mode	Test point	Signal

Diagnosis:

_____

_____

Corrective action:

_____

_____

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